

# **HANDBOOK OF SEMICONDUCTOR WAFER CLEANING TECHNOLOGY**

**Science, Technology,  
and Applications**

Edited by

**Werner Kern**

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**NOYES PUBLICATIONS**  
Westwood, New Jersey, U.S.A.

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Library of Congress Catalog Card Number: 93-4078

ISBN: 0-8155-1331-3

Printed in the United States

Published in the United States of America by  
Noyes Publications  
Fairview Avenue, Westwood, New Jersey 07675

10 9 8 7 6 5

Library of Congress Cataloging-in-Publication Data

Handbook of semiconductor wafer cleaning technology : science, technology, and applications / edited by Werner Kern.

p. cm.

Includes bibliographical references and index.

ISBN 0-8155-1331-3

1. Semiconductor wafers--Cleaning. I. Kern, Werner. 1925-

TK7871.85.H335 1993

93-4078

621.3815'2--dc20

CIP

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## **Part I.**

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# **Introduction and Overview**

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# Overview and Evolution of Semiconductor Wafer Contamination and Cleaning Technology

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***Werner Kern***

## 1.0 INTRODUCTION

### 1.1 Importance of Clean Wafer Surfaces

The importance of clean substrate surfaces in the fabrication of semiconductor microelectronic devices has been recognized since the dawn of solid-state device technology in the 1950s. It is well known that the device performance, reliability, and product yield of silicon circuits are critically affected by the presence of chemical contaminants and particulate impurities on the wafer or device surface. Effective techniques for cleaning silicon wafers initially and after oxidation and patterning are now more important than ever before because of the extreme sensitivity of the semiconductor surface and the submicron sizes of the device features. As a consequence, the preparation of *ultraclean* silicon wafers has become one of the key technologies in the fabrication of ULSI silicon circuits, such as 64- and 256-megabit DRAM devices. The term "ultraclean" may be defined in terms of the concentration of both chemical contaminants and particles on the silicon surface. Specifically, total metallic impurities should be, conservatively speaking, less than  $10^{10}$  atoms per  $\text{cm}^2$ . Particles larger than  $0.1\ \mu\text{m}$  in size should be fewer than approximately  $0.1$  per  $\text{cm}^2$ , which translates to fewer than 30 particles per 200 mm wafer. These extremely low numbers are impressive indeed! The reason for these stringent specifications is the fact that the overall device quality, as noted, is critically

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affected by trace impurities. Each of the hundreds of processing steps in the fabrication of advanced silicon circuits can contribute to contamination.

### **1.2 Wafer Cleaning Technology**

The objective of wafer cleaning is the removal of particulate and chemical impurities from the semiconductor surface without damaging or deleteriously altering the substrate surface. Dry-physical, wet-chemical, and vapor-phase methods can be used to achieve these objectives. An array of equipment is available for implementing the various processes for industrial applications.

Nearly all wafer cleaning processes have been developed specifically for silicon since silicon semiconductor devices are by far the most important industrially for the fabrication of integrated circuits (ICs). Special procedures must be used for germanium and compound semiconductor materials.

The traditional approach of wafer cleaning is based on wet-chemical processes, which use mostly hydrogen peroxide solutions. Successful results have been achieved by this approach for the past twenty-five years. However, the relatively large consumption of chemicals required by these processes, the disposal of chemical waste, and the incompatibility with advanced concepts in integrated processing (such as cluster tooling) are the main reasons why methods based on gas-phase cleaning are now being developed that are less affected by these limitations.

The development of wafer cleaning technology had a slow start in the early period of 1950 to 1970, but then accelerated with the refinements of semiconductor device architecture and the increasing criticalness of contaminant-free surfaces. The greatly increased level of research and development of improved and new cleaning processes, coupled with advances in analytical methodology and instrumentation for the detection and characterization of impurities and surface structures, has been especially pronounced for the past three years. This increased level of activity is exemplified by recent international conferences and symposia on wafer cleaning and related science and technology (1)-(8), and the appearance of several volumes on particle contamination (9)-(11).

### **1.3 Scope and Organization of This Chapter**

This chapter is intended as a general introduction to and overview of semiconductor wafer cleaning, as discussed in this book. There are many

important aspects and topics associated with this subject, both scientific and technological, that should be addressed to gain a well-rounded understanding of this important field of semiconductor processing. Details are kept to a minimum in this overview, except for some topics that merit special emphasis or that are not discussed elsewhere in this volume, since the various chapters treat the material in depth.

It is informative and interesting to review the development of wafer cleaning science and technology from the beginning to the present time. I have attempted to trace who has done what, when, and how, documenting the contributions in the literature references and stressing major achievements for proper perspective.

The chapter is divided into three main sections:

- Overview of wafer contamination aspects
- Overview of wafer cleaning technology
- Evolution of wafer cleaning science and technology

## **2.0 OVERVIEW OF WAFER CONTAMINATION ASPECTS**

### **2.1 Types and Origins of Contaminants**

Contaminants on semiconductor wafer surfaces exist as contaminant films, discrete particles or particulates (groups of particles) and adsorbed gases, as summarized in Table 1. Surface contaminant films and particles can be classified as molecular compounds, ionic materials, and atomic species. Molecular compounds are mostly particles or films of condensed organic vapors from lubricants, greases, photoresists, solvent residues, organic components from DI water or plastic storage containers, and metal oxides or hydroxides. Ionic materials comprise cations and anions, mostly from inorganic compounds that may be physically adsorbed or chemically bonded (chemisorbed), such as ions of sodium, fluorine and chlorine. Atomic or elemental species comprise metals, such as gold and copper, that may be chemically or electrochemically plated out on the semiconductor surface from hydrofluoric acid (HF)-containing solutions, or they may consist of silicon particles or metal debris from equipment.

The sources of contaminants are listed in Table 2 and are seen to be manifold. Particles can originate from equipment, processing chemicals, factory operators, gas piping, etc. Mechanical (moving) equipment and containers for wafers and liquids are especially serious sources, whereas

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materials, liquids, gaseous chemicals, and ambient air tend to cause less particle contamination, but all contribute significantly to the generation of contaminant films. Static charge built-up on wafers and carriers is a powerful mechanism of particle deposition that is often overlooked. The origins of particles in advanced integrated circuits (DRAMs or Dynamic Random Access Memory devices) are shown in Table 3 in terms of percent distribution of the total. As the complexities of the devices increase to the present 16-Mbit types and to the future 64-Mbit types, the distribution shifts as indicated.

**Table 1. Forms and Types of Contaminants**

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<b>▲ Equipment:</b>	Mechanical Deposition systems Ion implanters	Gas piping Metal tweezers Liquid-containers
<b>▲ Humans:</b>	Factory operators Process engineers	
<b>▲ Materials:</b>	Liquid chemicals Etchants D.I. water	Photoresists Air Gasses
<b>▲ Processes:</b>	Combination of all above sources	

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**Table 2. Sources of Particles and Contaminant Films**

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<b>▲ Forms:</b>	Films, discrete particles, particulates, micro-droplets, vapors and gases
<b>▲ Types:</b>	Molecular, ionic, atomic, gaseous
<b>▲ Ionic:</b>	Physisorbed and chemisorbed cations and anions from inorganics; e.g. $\text{Na}^+$ , $\text{Cl}^-$ , $\text{SO}_4^{2-}$ , fluoride species
<b>▲ Atomic:</b>	Elemental metal films and particles; e.g. electrochemically plated Au, Ag, Cu films; particles of Si, Fe, Ni
<b>▲ Gaseous:</b>	Adsorbed gases and vapors; generally of little practical consequence

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**Table 3.** Distribution of Particle Defects ( $>0.5\ \mu\text{m}$ ) in DRAMs. (Source: Lam Research Corp. 1990.)

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<i>Particle Origin</i>	<i>% Distribution in DRAMs</i>			
	<i>1-Mbit</i>	<i>4-Mbit</i>	<i>16-Mbit</i>	<i>64-Mbit</i>
▲ Tools	40	40	35	25
▲ Process	25	25	40	60
▲ Environment	25	25	15	10
▲ Handling	10	10	10	5

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## 2.2 Types of Semiconductor Wafers

The vast majority of semiconductor wafers used in the fabrication of solid-state microelectronic devices are silicon. However, a small fraction of all wafers are compound semiconductors, such as gallium arsenide, gallium phosphide, and numerous complex alloys. The importance of these materials has grown steadily for unique applications in opto-electronics. The great differences in chemical properties between these semiconductors and those of silicon require different and specialized cleaning treatments. Published information on cleaning of compound semiconductor wafers is scarce and, therefore, has to be restricted in this chapter (and in the book as a whole) to limited comments whenever possible.

Semiconductor wafers can be in the form of mechanically lapped and chemo-mechanically polished slices cut from single-crystal ingots. They may be coated with an epitaxial layer of the semiconductor with different dopant type and concentration, or they may be coated with a film of uniform or patterned silicon dioxide. Up to this point in the processing, wafer cleaning operations can utilize highly reactive chemicals that do not attack these corrosion-resistant materials. The situation changes drastically once layers or patterns of deposited metals are present on the wafers. The cleaning chemistry must then be confined to mild and noncorrosive treatments, such as rinses with dilute acids, de-ionized (DI) water, and selected organic solvents.



**2.3 Effects of Contaminants on Semiconductor Devices**

The effects of contaminants on semiconductor materials and dielectrics during wafer processing, and the effects on the finished semiconductor devices, are complex and depend on the nature and quantity of a specific type of contaminant. The importance of their control and minimization is obvious from the fact that over fifty percent of the yield losses in IC manufacturing are caused by microcontamination. A selection of representative papers published from 1987 to 1992 on this important subject is included as Refs. 12 - 31. A brief summary of contamination effects is presented in Table 4.

**Table 4. Effects of Contaminants**

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<b>▲ Molecular types:</b>	Block and mask operations Impair adhesion Form deleterious decomposition products Nucleate defects in films
<b>▲ Ionic types:</b>	Diffuse on surface, in bulk, at interfaces Cause electrical device defects Degrade device performance and yield Cause crystal defects Lower oxide breakdown field
<b>▲ Atomic types:</b>	Can diffuse readily Cause surface conduction Decrease minority-carrier lifetime Degrade electrical device performance Lower product yield Nucleate crystal defects Particles short-out conductor lines

---

Molecular contaminant films on wafer surfaces can prevent effective cleaning or rinsing, impair good adhesion of deposited films, and form deleterious decomposition products. For example, organic residues, if heated to high temperatures in a non-oxidizing atmosphere, can carbonize and, in the case of silicon wafers, form silicon carbide that can nucleate polycrystalline regions in an epitaxial deposit.

Ionic contaminants cause a host of problems in semiconductor devices. During high-temperature processing, or on application of an electric field, they may diffuse into the bulk of the semiconductor structure or spread on the surface, leading to electrical defects, device degradation, and yield losses. For example, highly mobile alkali ions in amorphous  $\text{SiO}_2$  films on Si may cause drift currents and unstable surface potential, shifts in threshold and flat-band voltages, surface current leakage, lowering of the oxide breakdown field of thermally grown films of  $\text{SiO}_2$ , etc. In the growth of epitaxial silicon layers, sufficiently high concentrations of ions can give rise to twinning dislocations, stacking faults, and other crystal defects.

Certain metallic contaminants are especially detrimental to the performance of semiconductor devices, as indicated in Table 5. Since silicon is above hydrogen in the electromotive series of the elements, heavy metals tend to deposit from solution on its surface by galvanic action, actually plating out with high efficiency, especially from HF-containing etchants. If not removed, these impurities may diffuse into the silicon substrate during later heat treatments and introduce energy levels into the forbidden band to act as traps or generation/recombination centers, cause uncontrolled drifts in the semiconductor surface potential, affect the surface minority-carrier lifetime and the surface recombination velocity, lead to inversion or accumulation layers, cause excessive leakage currents, and give rise to various other device degradation and reliability problems. Metal contaminants in or on semiconductor wafers can lead to structural defects in vapor-grown epitaxial layers and degrade the breakdown voltage of gate oxides.

**Table 5.** Impurity Elements

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The following common impurity elements from chemicals and processing can be deleterious to silicon devices:

▲ **Heavy metals (most critical)**

Fe, Cu, Ni, Zn, Cr, Au, Hg, Ag

▲ **Alkali metals (critical)**

Na, K, Li

▲ **Light elements (less serious)**

Al, Mg, Ca, C, S, Cl, F

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Particles can cause blocking or masking of wafer processing operations, such as photolithography, etching, deposition, and rinsing. They may obstinately adhere to surfaces by electrostatic adsorption and may become embedded during film formation. Deposition and removal of particles becomes exacerbated as the size decreases because of the extremely strong adhesion forces. Furthermore, particles constitute a potential source of chemical contamination, depending on their composition. Particles that are present during film growth or deposition can lead to pinholes, microvoids, microcracks, and the generation of defects as noted above, depending on their chemical composition. In later stages of device fabrication, particles can cause shorts between conductor lines if they are sufficiently large, conductive, and located adjacently between conductor lines. They are considered potential device killers if their size is larger than one tenth the size of the minimum size feature of the particular integrated circuit.

Adsorbed gases and moisture have much less serious effects, but they can cause problems by outgassing in vacuum systems and affecting the quality of deposited films.

### 2.4 Prevention of Contamination from Equipment and Processing

Semiconductor surface microcontamination and its control (9), prevention, detection, and measurement are topics that may seem beyond the scope of wafer cleaning. However, these aspects are intimately interconnected with wafer cleaning and are, therefore, included briefly in this chapter and more extensively in several chapters of the present volume.

The key notion of this topic is *prevention*. If we can prevent contamination during the entire semiconductor device manufacturing process by creating and maintaining super-clean conditions in equipment, materials, and environment, there would be little need for wafer cleaning. Furthermore, it is generally easier (or less difficult!) to prevent contamination rather than to remove it once it has taken place. Therefore, avoiding contamination must be the first priority, and strict contamination control should be exercised to the fullest extent throughout device manufacturing (32). Changes in contamination control requirements have been reassessed recently (17)(33).

Processing equipment has been the major source of particle contamination (34) and must be controlled effectively by eliminating dust particles through scheduled maintenance and by electrostatic charge removal (34). Particle generation can be further minimized by eliminating friction of moving equipment parts, avoidance of turbulent gas flows, reduction of operator handling through automation, and by exercising periodic cleanup actions (35).

Next to equipment, semiconductor wafer processing in the fab must be controlled. Carefully optimized processing conditions for film deposition, plasma etching, ion implantation, thermal treatments, and other critical processing steps are effective measures for preventing particle deposition. For example, in chemical vapor deposition, particle-generating homogeneous gas-phase nucleation must be minimized by optimizing the reaction parameters. Recirculation of the partially depleted reaction gases must be avoided by improved equipment design. Sudden bursts in the introduction of gases into a system should be prevented by using "soft starts" to gradually increase the gas flow rates, and so forth (36).

## **2.5 Purity of Chemicals (37)**

Many chemicals are used in the fabrication of semiconductor devices and impurities in those chemicals can critically affect the quality of the devices. Stringent control must be imposed to minimize contamination by transfer of impurities from these sources. Most chemicals used in wafer processing are either gases or liquids. Gases are obtainable at very high purity and can be ultra-filtered relatively easily to remove particles quite effectively. Liquid processing chemicals are numerous, as shown in the compilation of Table 6.

Impurity levels in chemicals can be quite variable. A list of trace metals found in several liquid chemicals of typical electronic purity grade is presented in Table 7 as an example. It can be seen that the impurity concentrations vary considerably for any one chemical, depending on its source. Great efforts have been made in recent years by the producers of chemicals to provide the electronics industry with *ultrapure* materials (7)(38)-(40). "Ultrapure" can be defined as meaning total impurity concentrations in the low ppb (parts per billion) range. A more restricted alternative for producing ultrapure acids is the point-of-use generation with reproprocessors (41)(42).

The method of dispensing can affect the particle concentration very significantly, as exemplified by the results in Table 8 where bulk-distributed chemicals are compared with their bottle-dispensed counterparts. The latter exhibit very high particle counts from recontamination during the dispensing step. This secondary type of contamination of originally ultrapure chemicals that is introduced from containers, pipes, valves, etc. has been a serious and often neglected problem that demands stringent control (38)(39).

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**Table 6.** Liquid Chemicals in the Semiconductor Industry

▲ Acids	▲ Alkalis	▲ Resist chemicals
HF	NH <sub>4</sub> OH	Resist preparations
H <sub>2</sub> SO <sub>4</sub>	KOH	Developers
HCl	NaOH	Solvents
H <sub>3</sub> PO <sub>4</sub>	Choline	Strippers
HNO <sub>3</sub>	Tertiary amines	Adhesion promoters
CH <sub>3</sub> CO <sub>2</sub> H		Coupling agents
▲ Solvents	▲ Reactants	▲ Organometallics of
Isopropanol	H <sub>2</sub> O <sub>2</sub>	Si, Ge
Ethanol	NH <sub>4</sub> F	B, P, As, Sb
Trichloroethylene	SiCl <sub>4</sub>	Al, Cu, Ga, In
Acetone	SiHCl <sub>3</sub>	Ta, Nb
Toluene	Si(C <sub>2</sub> H <sub>5</sub> O) <sub>4</sub>	▲ Universal
Ethylacetate	Br	D.I. Water
Methylene chloride	EDTA	
Freons	Surfactants	

**Table 7.** Trace Metallic Impurities in some Liquid Chemicals. (Source: Balazs Analytical Labs.)

<i>Chemical</i>	<i>No. Brands</i>	<i>No. Metals</i>	<i>ppb Range</i>
H <sub>2</sub> O <sub>2</sub>	5	30	6.2-160
HF	5	30	25-133
IPA	2	26	44, 184
MeOH	2	26	100, 184
H <sub>2</sub> SO <sub>4</sub>	6	30	28-246
HCl	5	30	81-470
Acetone	2	26	30, 1,043
Resists	5	16	430-1,400
Strippers	7	17	264-4,945

**Table 8.** Bulk-Distributed vs. Bottled Chemicals. (Source: Grant and Schmidt, FSI)

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<b>▲ Bulk,*</b> <i>op. hrs</i>	<i>&gt;0.5<math>\mu</math>m Particles per mL</i>			
	<i>H<sub>2</sub>SO<sub>4</sub></i>	<i>NH<sub>4</sub>OH</i>	<i>H<sub>2</sub>O<sub>2</sub></i>	<i>HCl</i>
0.1	27	28	0.06	0.02
1.0	7.0	1.9	0.03	0.01
8.0	2.0	0.17	0.02	<0.01
<b>▲ Bottled**</b>	60	500	100	40

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\* FSI Chemfill™

\*\* Clearroom™ Low-particle, 1 gallon bottle, Ashland Chemical Company

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An interesting approach to circumvent these difficulties is in situ generation of aqueous chemicals by use of high-purity DI water and reactant gases, such as ozone (43)-(45), HCl, and NH<sub>3</sub> (45).

De-ionized water, which could be considered the primary chemical, is used widely as a diluent, cleaning chemical, and rinsing agent in many wafer cleaning process steps. Chemical impurities, organics, and particles in DI water must also be carefully controlled to prevent contamination of the semiconductor wafers (38)(46)(47). Typical impurity levels of ultrapure DI water are compared with those of high-purity sulfuric acid and hydrofluoric acid in Table 9.

In summary, it can be said that ultrapure, low-particulate chemicals, organic solvents, and DI water, should be used for all critical wafer processing operations. High-purity gas, water, and chemical bulk-distributed delivery subsystems with point-of-use ultra-filtration should be installed in the fabrication areas to eliminate particle-generating dispensing from individual source containers. In situ generation of aqueous chemicals should be implemented whenever possible.

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**Table 9.** Impurities in Chemicals vs. Water in 1991. (Source: Millipore Corp.)

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	<i>98% H<sub>2</sub>SO<sub>4</sub></i>	<i>49% HF</i>	<i>Ultrapure Water</i>
▲ Particles (≥0.2μm)	100-500 per mL	10-50 per mL	6 per mL
▲ Individual metal ions	1-5 ppb	1 ppb	<0.1 ppb
▲ Total metal ions	≤70 ppb	≤40 ppb	<1 ppb

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### 2.6 Analytical Methods

Another important aspect of contamination control that can only be briefly discussed is the analytical methodology for measuring and monitoring trace and ultra-trace levels of impurities and particles in processing reactants, DI water, gases, and the ambient air in processing areas on the one hand, and on the semiconductor wafer surface on the other. Analysis and measurement of contaminants in source materials and on the wafer surface are needed in establishing process conditions to identify what specific impurities are transferred during processing to the critical semiconductor surface and at what concentration. This information is the first step to be taken in improving a process to attain ultraclean wafers. On-line, in situ analytical testing is desirable in many critical operations to continuously monitor the concentration of specific contaminants such as particles, gaseous species, moisture, or metal ions so as to allow real-time process control (48).

Impressive progress has been made in recent years in increasing the sensitivity and speed of non-destructive instrumental analysis methods for ultra-trace impurities on surfaces. Outstanding examples are secondary ion mass spectroscopy (SIMS) and total reflection x-ray fluorescence (TXRF) analysis, both combined with vapor-phase decomposition techniques to

concentrate the impurities. These advanced methods of analysis now offer detection capabilities down to an astonishing  $10^7$  to  $10^8$  metal atoms per  $\text{cm}^2$ . Volume-sensitive methods for bulk contamination analysis of semiconductors have also been refined or developed, such as surface photovoltage (SPV) for measuring minority-carrier diffusion length, and deep-level transient spectroscopy (DLTS) for lifetime measurements (49)-(56).

The atomic structure and morphology of semiconductor surfaces after various chemical treatments has been studied by diffraction, imaging, and vibrational methods. These sophisticated techniques of analysis are discussed in Ch. 10 on surface chemical composition and morphology. An excellent example of applications of some of these methods (including x-ray photoelectron spectroscopy, high resolution electron energy-loss spectroscopy, and angle resolved light scattering) has been published in Ref. 57.

### **3.0 OVERVIEW OF WAFER CLEANING TECHNOLOGY**

#### **3.1 Approaches for Attaining Clean Semiconductor Wafers**

A combination of several approaches should be used for most effectively achieving the required high level of cleanliness of the semiconductor surface:

1. Control and prevention of contamination from processing equipment and chemicals
2. Removal of wafer contaminants by liquid cleaning methods
3. Removal of wafer contaminants by gas-phase cleaning methods

The first approach is applicable to all processing steps in the manufacture of semiconductor devices and has been discussed in Sec. 2.4. The contaminant removal methods noted in items 2 and 3 refer specifically to wafer cleaning steps prior to metal deposition and are reviewed in this section. References are representative rather than comprehensive, and the most recent advances will be discussed in more detail in Sec. 4.4.

#### **3.2 Liquid Cleaning Methods**

Liquid cleaning refers to processes that use liquid cleaning reagents or mixtures. They are usually, but not always, chemical in nature and are



based on water as the liquid component, hence the more popular but incorrect term *wet-chemical*. Cleaning with organic solvents is neither chemical nor wet. Cleaning with aqueous oxidizing agents, on the other hand, is true wet-chemical.

The mechanism of liquid cleaning can be purely physical dissolution and/or chemical reaction dissolution. Chemical etching occurs when materials are removed by a chemical transformation to soluble species. Traditionally, chemical etching is expected to remove substantial quantities of a material, such as a deposited film on a substrate. Some chemical dissolution reactions may result in the removal of only a few atomic layers of material, and by above definition should be considered chemical etching processes; perhaps the term *microetching* should be used for such processes, which actually occur in most wet-chemical wafer cleaning processes.

Conventional wet-chemical etching processes for the removal of bulk quantities of electronic materials are beyond the scope of this book. Several comprehensive reviews have been published that cover this topic thoroughly (58)-(61).

Liquid cleaning methods for semiconductor wafers are based on the application of mineral acids, aqueous solutions including DI water, hydrogen peroxide containing mixtures, and organic solvents. The requirements for a typical wafer cleaning process are outlined in Table 10. Different process combinations and sequences are used for specific applications. A variety of technical equipment is available commercially for efficiently implementing cleaning processes for high-volume fabrication of ICs. Rinsing, drying, and storing of cleaned wafers is intimately connected with cleaning operations and is also addressed in the section that follows.

Organic solvents are rarely used for cleaning pre-metallized silicon wafers where much more effective cleaning agents can be used. Compound semiconductor wafers, however, are frequently treated with organic solvents to attain some degree of cleaning, since suitable and safe wet-chemical cleans cannot always be used or may not be available. Chlorofluorocarbon compounds, acetone, methanol, ethanol, and isopropyl alcohol (IPA) are solvents that are frequently used to remove organic impurities. IPA is generally the purest organic solvent available, as seen from Table 7, and is used extensively for vapor drying of water-rinsed wafers. Chlorofluorocarbon solvents are being phased out rapidly because of ecological problems related to ozone destruction.

**Table 10.** Requirements for a Silicon Wafer Cleaning Process

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1. Effective removal of all types of surface contaminants
  2. Not etching or damaging Si and SiO<sub>2</sub>
  3. Use of contamination-free and volatilizable chemicals
  4. Relatively safe, simple, and economical for production applications
  5. Ecologically acceptable, free of toxic waste products
  6. Implementable by a variety of techniques
- 

### **3.3 Wet-Chemical Cleaning Processes**

**Hydrofluoric Acid Solutions.** Mixtures of concentrated hydrofluoric acid (49 wt% HF) and DI water have been widely used for removal by etching of silicon dioxide (SiO<sub>2</sub>) films and silicate glasses (e.g., phosphosilicates, borophosphosilicates) that were grown or vapor deposited on semiconductor substrate wafers (58)(59). The chemical dissolution reactions have been identified and described in the literature and are discussed in Chs. 7 and 10.

The thin layer of native oxide on silicon, typically 1.0 to 1.5 nm thick, is removed by a brief immersion of the wafers in diluted (typically 1:50 or 1:100) ultrapure filtered HF solution at room temperature. The change of the wetting characteristics of the initially hydrophilic surface to a hydrophobic surface, which strongly repels aqueous solutions, indicates when the oxide dissolution is complete. The effect is due to the hydrogen-passivated silicon surface that results from exposure to HF solutions. The resulting hydrogenated silicon surface is highly sensitive to oppositely charged particles in solution, and also to organic impurities from DI water and ambient air that are strongly attracted to the surface. Treatments with HF

solutions that leave the semiconductor surface bare must, therefore, be carried out with ultrapure and ultra-filtered HF solution in a very clean atmosphere. In addition to being an etchant for oxides and silicates, HF solutions desorb certain metallic impurities from the surface. On the other hand, they tend to contaminate silicon with iron deposits. The primary purpose of HF treatments, however, is to expose the silicon surface to subsequent attack by other cleaning agents, such as in an  $\text{H}_2\text{O}_2$ -based cleaning sequence (62)(63).

Mixtures of hydrofluoric acid and ammonium fluoride ( $\text{NH}_4\text{F}$ ) are known as buffered oxide etch (BHF) and are used for pattern delineation etching of dielectric films to avoid loss of the photoresist polymer pattern that would not withstand the strongly acidic HF solution without a buffering agent. Whereas the free acid is the major etching species in aqueous HF solutions, the ionized fluoride associate  $\text{HF}_2^-$  is the major etchant species in buffered HF solutions. Addition of  $\text{NH}_4\text{F}$  increases the pH to 3 - 5, maintains the concentration of fluoride ions, stabilizes the etching rate, and produces the highly reactive  $\text{HF}_2^-$  ions. A commonly used BHF composition of 7:1  $\text{NH}_4\text{F}$  (40%)-HF (49%) has a pH of about 4.5 and appears to contain only  $\text{HF}_2^-$  and  $\text{F}^-$ , with very little free HF acid. The  $\text{SiO}_2$  etching rate of  $\text{HF}_2^-$  is four to five times as fast as that for the HF species in aqueous hydrofluoric acid (59). Additional details of the chemistry involved in these reactions (and of wet-chemical etching in general) can be found in Refs. 58 and 59. The subtle differences in the silicon surface morphology resulting from these two types of etchants are discussed in detail in Ch. 10.

Very recent references on acid etchants ( $\text{H}_2\text{O}$ - $\text{H}_2\text{O}_2$ -HF,  $\text{HNO}_3$ -HF) and very dilute acids ( $1:10^3$  -  $1:10^6$ ) for silicon cleaning are described in Sec. 4.4.

**Sulfuric-Acid/Hydrogen-Peroxide Mixtures.** Removal of heavy organic materials from silicon wafers, such as photoresist patterns and other visible gross contaminants of organic nature, can be accomplished with mixtures of 98%  $\text{H}_2\text{SO}_4$  and 30%  $\text{H}_2\text{O}_2$ . Volume ratios of 2 - 4:1 are used at temperatures of 100°C and above. A treatment of 10 - 15 min at 130°C is most effective, followed by vigorous DI water rinsing to eliminate all of the viscous liquid. Organics are removed by wet-chemical oxidation, but inorganic contaminants, such as metals, are not desorbed. These mixtures, which are also known as "piranha etch" (because of their voracious ability to eradicate organics) or, incorrectly, "Caros acid", are extremely dangerous to handle in the fab; goggles, face shields, and gloves are needed to protect the operators. Finally, it is advantageous after the

rinsing to strip the impurity-containing oxide film on silicon or on the thermal  $\text{SiO}_2$  layer by dipping the wafers for 15 sec in 1%  $\text{HF-H}_2\text{O}$  (1:50), followed by a DI water rinse (62)(63).

**Conventional RCA-Type Hydrogen Peroxide Mixtures (62)-(64).**

These are the most widely used and best established cleaning solutions for silicon wafers. They are made up of ultra-filtered, high-purity DI water, high-purity "not stabilized" hydrogen peroxide, and either electronic-grade ammonium hydroxide or electronic-grade hydrochloric acid. The hydrogen peroxide must be very low in aluminum and stabilizer additives (sodium phosphate, sodium stannate, or amino derivatives) to prevent wafer recontamination. These mixtures, used in two process steps, have become known as RCA standard cleans (SC-1 and SC-2). The treatment is usually preceded by the preliminary cleaning described in the previous section. The development of the *original* SC-1 and SC-2 mixtures is described in Section 4.2. Tables 11 and 12 summarize the salient features of these two solutions.

The first step uses a mixture (SC-1) of 5:1:1 vol. DI water,  $\text{H}_2\text{O}_2$  (30%, "not stabilized"), and  $\text{NH}_4\text{OH}$  (29 w/w% as  $\text{NH}_3$ ) at  $70^\circ\text{C}$  for 5 min, followed by quench and rinse with cold ultra-filtered DI water. This deceptively simple procedure removes any remaining organics by oxidative dissolution. Many metal contaminants (group IB, group IIB, Au, Ag, Cu, Ni, Cd, Co, and Cr) are dissolved, complexed, and removed from the surface.

**Table 11.** Cleaning Processes Based on Diluted Mixtures of  $\text{H}_2\text{O}_2$  and  $\text{NH}_4\text{OH}$  or  $\text{HCl}$

- 
- ▲ First systematically developed wafer cleaning process for bare and oxidized Si. Introduced to RCA device fabrication in 1965, published in 1970.
  - ▲ RCA cleaning process is based on a 2-step wet-oxidation and complexing treatment in aqueous  $\text{H}_2\text{O}_2$ -  $\text{NH}_4\text{OH}$  and  $\text{H}_2\text{O}_2$  -  $\text{HCl}$  mixtures at  $75$ - $80^\circ\text{C}$  for 10 min.
  - ▲ Chemical Principles:
    1.  $\text{H}_2\text{O}_2$  at high pH is a powerful oxidant, decomposing to  $\text{H}_2\text{O} + \text{O}_2$
    2.  $\text{NH}_4\text{OH}$  is a strong complexant for many metals
    3.  $\text{HCl}$  in  $\text{H}_2\text{O}_2$  forms soluble alkali and metal salts by dissolution and/or complexing
    4. Mixtures formulated not to attack Si or  $\text{SiO}_2$
-

**Table 12. Original RCA Cleaning Solutions**


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<b>Step 1</b>
<ul style="list-style-type: none"> <li>▲ "Standard Clean 1 or SC-1", alkaline peroxide mixture consisting of 5 vol H<sub>2</sub>O + 1 vol H<sub>2</sub>O<sub>2</sub> 30% + 1 vol NH<sub>4</sub>OH 29%, followed by D.I. water rinse</li> <li>▲ Effects wet oxidation removal of organic surface films and exposes the surface for desorption of trace metals (Au, Ag, Cu, Ni, Cd, Zn, Co, Cr, etc.)</li> <li>▲ Keeps forming and dissolving hydrous oxide film</li> </ul>
<b>Step 2</b>
<ul style="list-style-type: none"> <li>▲ "Standard Clean 2 or SC-2", acidic peroxide mixture consisting of 6 vol H<sub>2</sub>O + 1 vol H<sub>2</sub>O<sub>2</sub> 30% + 1 vol HCl 37%, followed by D.I. water rinse</li> <li>▲ Dissolves alkali ions and hydroxides of Al<sup>3+</sup>, Fe<sup>3+</sup>, Mg<sup>2+</sup></li> <li>▲ Desorbs by complexing residual metals</li> <li>▲ Leaves protective passivation hydrated oxide film</li> </ul>

---

The solution temperature should be 70°C for sufficient thermal activation, but must not exceed 80°C to avoid excessively fast decomposition of the H<sub>2</sub>O<sub>2</sub> and loss of NH<sub>3</sub>. The treatment is terminated by, ideally, an overflow quench with cold DI water to displace the surface layer of the liquid and to reduce the temperature to prevent any drying of the wafers on withdrawal from the bath.

SC-1 slowly dissolves the thin native oxide layer on silicon and forms a new one by oxidation of the surface. This oxide regeneration has a self-cleaning effect and aids the removal of particles by dislodging them. These effects account undoubtedly for some of the beneficial results achieved by the treatment.

SC-1 also etches silicon at a very low rate. The standard 5:1:1 composition can have a surface roughening effect due to non-uniform local micro-etching. Lower fractions of NH<sub>4</sub>OH have been proposed to avoid micro-roughening of the silicon, as further discussed in Sec. 4.4.

The second step in the conventional RCA cleaning procedure uses a mixture (SC-2) consisting of 6:1:1 vol. DI water, H<sub>2</sub>O<sub>2</sub> (30%, "not stabilized"),

and HCl (37 w/w%). A solution temperature of 70°C for 5 - 10 minutes is used, followed by quenching and rinsing as in the SC-1 treatment. SC-2 removes alkali ions,  $\text{NH}_4\text{OH}$ -insoluble hydroxides such as  $\text{Al}(\text{OH})_3$ ,  $\text{Fe}(\text{OH})_3$ ,  $\text{Mg}(\text{OH})_2$ , and  $\text{Zn}(\text{OH})_2$ , and any residual trace metals (such as Cu and Au) that were not completely desorbed by SC-1.

SC-2 does not etch oxide or silicon, and does not have the beneficial surfactant activity of SC-1. Redeposited particles are, therefore, not removed by this mixture. The exact composition of SC-2 is much less critical than that of SC-1. The solution has better thermal stability than SC-1, and thus the treatment temperature need not be controlled as closely.

An optional etching step with dilute HF solution can be used between the SC-1 and SC-2 treatments of bare silicon wafers. Since the hydrous oxide film from the SC-1 treatment may entrap trace impurities, its removal before the SC-2 step should be beneficial. A 15-second immersion in 1% HF- $\text{H}_2\text{O}$  (1:50) solution is sufficient to remove this film, as evidenced by the change from the hydrophilic oxidized surface to hydrophobic after stripping. However, unless high-purity and point-of-use ultra-filtered and particle-free HF solution is used under controlled conditions, recontamination will result. A silicon surface that was exposed to HF solution immediately attracts particles and organic contaminants from solutions, DI water, and the ambient air, as noted before. In contrast to SC-1, the subsequent SC-2 solution does not release these contaminants. It may therefore be preferable to rely on the dissolution and regrowth action of SC-1. If a pre-clean is used, then the 1% HF step *prior* to SC-1 is recommended, since SC-1 will remove most particles and other contaminants. Exposure of bare silicon wafers to HF solution after SC-2 is generally not advisable since it would cause loss of the protective oxide film that passivates the silicon surface.

**Choline Solutions.** Choline is trimethyl-2-hydroxyethyl ammonium hydroxide and can be used as a replacement of inorganic bases for etching and cleaning. It is a strong and corrosive base without alkali elements and etches silicon like other bases. A formulation of the chemical is available commercially (Summa-Clean SC-15M, Mallinckrodt) which is a diluted choline solution containing a surfactant and methanol. Bulk etching of silicon can be prevented by adding  $\text{H}_2\text{O}_2$  as an oxidant (65). This mixture, which has excellent wetting characteristics for silicon wafers (66), is similar to SC-1 in its effect. In fact, some researchers have found it more efficient than SC-1 and other pre-oxidation cleans (67). Despite the fact that choline has been examined for many years, there is relatively little published information available, most data being contained in proprietary technical

reports, sometimes with contradictory results. An automatic dual-cassette spray machine that uses a warm choline- $\text{H}_2\text{O}_2$ - $\text{H}_2\text{O}$  mixture and a DI water spray rinse is available commercially (68). In some procedures the mixture replaces only SC-1 in the RCA cleaning procedure.

### 3.4 Implementation of Wet-Chemical Cleaning Processes

The processes described in the preceding sections can be implemented in the fab by the following techniques (63):

1. Immersion tank technique (Table 13)
2. Centrifugal spraying (Table 14)
3. Megasonic processing (Table 15)
4. Closed system method (Table 16)
5. Brush scrubbing for hydrodynamically removing large particles from wafers with special brushes and DI water or isopropyl alcohol.
6. High-pressure fluid jet cleaning with a potentially harmful high-velocity jet of liquid sweeping over the surface at pressures of up to 4000 psi (68).

Detailed descriptions of these techniques are included in Chs. 3 and 4.

**Table 13.** Immersion Tank Technique

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- ▲ Original technique for RCA cleaning process
  - ▲ Vessels of fused silica used with SC-1, SC-2 to prevent leaching of Al, B, Na from Pyrex. (Polypropylene vessel for optional HF- $\text{H}_2\text{O}$ ).
  - ▲ Batch of wafers immersed in SC-1 followed by water rinse and SC-2 for each 10 min at 75-80°C
  - ▲ Reactions terminated by overflow quenching with cold, ultrafiltered D.I. water followed by drying
  - ▲ Refined wet bench production systems are commercially available
-

**Table 14. Centrifugal Spraying**

- 
- ▲ First automatic centrifugal spray cleaning machine for corrosives introduced in 1975 by FSI
  - ▲ Wafers rotate past stationary spray column
  - ▲ Filtered solutions, including HF-H<sub>2</sub>O, hot SC-1 and SC-2, are dispensed as spray onto spinning wafers
  - ▲ Solutions are freshly mixed just before spraying; reduced volumes are adequate
  - ▲ Faster than immersion techniques. Wafers remain enclosed for cleaning, rinsing, and spin drying.
  - ▲ Cleaning efficiency comparable with immersion technique, but particles are removed more efficiently
  - ▲ Centrifugal spray machines are maintenance extensive
- 

**Table 15. Megasonic Processing**

- 
- ▲ Developed at RCA for removing particles on wafers to complement peroxide immersion cleaning process.
  - ▲ Megasonics: A highly effective non-contact scrubbing method with high-pressure waves in a cleaning solution.
  - ▲ Achieved by ultrahigh frequency sonic energy at 0.85 - 0.90 MHz, generated by array of piezoelectric transducers.
  - ▲ Particles of 0.1  $\mu\text{m}$  to several microns are removed from front and backside of wafers with input power densities of 5-10 W/cm<sup>2</sup>; (ultrasonics at 20-80 kHz requires up to 50% higher power densities and is less effective for small particles).
  - ▲ Megasonics with SC-1 at 35-42°C simultaneously removes particles and contaminant films. Chemisorbed inorganics require higher temperatures (70°C) for complete desorption with SC-1/SC-2.
  - ▲ Commercial megasonic systems available from Vertec and Semiconductor Technologies.
-



**Table 16.** Closed System Method by Liquid Displacement

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- ▲ System developed in 1986 by CFM Technology ("Full Flow"™)
  - ▲ Keeps wafers enclosed and stationary during entire cleaning, rinsing, and drying cycle
  - ▲ Vessel containing wafer batch is hydraulically controlled to remain filled with hot or cold process fluids that flow sequentially and continuously over wafers in cassette
  - ▲ Repeated crossing through gas/liquid phase boundaries is avoided, thus eliminating recontamination of wafers that occurs on conventional pullout from immersion tank
- 

### 3.5 Wafer Rinsing, Drying, and Storing

The last steps in wet-chemical wafer cleaning are rinsing and drying (69)(70); both are extremely critical because clean wafers become recontaminated very easily. Rinsing should be done with flowing high-purity and ultra-filtered high-resistivity DI water, usually at room temperature. The results of several recent studies have been published (28)(71)-(73). Megasonic rinsing is advantageous (72) and is the most effective technique for reducing the critical boundary layer between the wafer surface and the rinse water (73). Centrifugal spray rinsing (74) and rinsing in a closed system (75) have the advantage that the wafers are not removed between cleaning, rinsing, and drying.

Wafer drying after rinsing should be done by physical removal of the water rather than by allowing it to evaporate. Spin drying accomplishes this and has been the most widely used technique, although recontamination occurs frequently. Filtered hot forced air or nitrogen drying is a preferred technique with less chance for particle recontamination (76)(77). Capillary drying is based on capillary action and surface tension to remove the water. Individual wafers are pulled out of DI water at 80 - 85°C; less than 1% of the water is said to evaporate, leaving a particle-free surface (69).

In solvent vapor drying, wet wafers are moved into the hot vapor of a high-purity water-miscible solvent, usually IPA (isopropyl alcohol), which condenses and displaces the water. The wafers dry particle-free when the cassette is withdrawn above the vapor zone. Commercial drying systems

for IPA and for non-flammable solvent mixtures are available (69)(75). The purity of the solvent is extremely important, and the water content during processing must be closely controlled so as not to exceed a critical concentration to achieve an ultraclean surface (69)(78)-(81). A comparative evaluation of spin rinse/drying and IPA vapor drying has been published recently (82). IPA on silicon surfaces could not be detected by SIMS, but the growth rate of native oxide films was depressed, indicating the presence of a thin IPA film; the electrical properties of the oxide improved substantially (83).

A recently developed technique of drying is known as "Marangoni drying". During removal of the wafer from the DI rinse water, the air-water-silicon surface is exposed to a stream of water-miscible organic solvent vapor. Surface tension effects cause the water to sheet off a planar wafer surface (84), leaving a very dry hydrophilic silicon surface. Finally, a novel low-pressure cleaning technique has been described recently (85).

Extreme care must be taken to avoid recontamination of clean device wafers during storage if immediate continuation of processing is not possible. Wafers should be placed, preferably, in a chemically-cleaned closed glass container or in a stainless steel container flushed with high-purity filtered nitrogen and stored in a clean room. Metal tweezers must never be used to handle semiconductor wafers since this will invariably cause contamination by traces of metals. The final criterion of the success of all wafer cleaning operations is the purity of the wafer surface after the last treatment. No matter how effective the various cleaning steps may be, improper rinsing, drying, and storage can ruin the best results (63).

### 3.6 Vapor-Phase Cleaning Methods

**General Considerations.** Vapor-phase cleaning is often called *dry cleaning* in contrast with *wet cleaning*. However, just like liquid cleaning is a more accurate term than the more restricted "wet cleaning" term, vapor-phase cleaning is a more correct expression than "dry-cleaning" since these processes are carried out in the gas or vapor phase, which are not necessarily dry. As noted in Sec. 1.1, vapor-phase cleaning has many actual and potential advantages over liquid cleaning methods in the fabrication of advanced semiconductor devices. Its development for commercial application is, as a consequence, being pursued vigorously. In this section we present a broad classification of vapor-phase cleaning processes and discuss some basic approaches for the removal of various groups of contaminant types. Referenced details have been included in Sec. 4.

**Classification of Vapor-Phase Cleaning Methods.** First, the impurities and contaminants on semiconductor wafers that must be removed by any method can be listed as follows:

1. Gross and trace organics
2. Native and chemical thin films of oxides
3. Physically and chemically adsorbed ions
4. Deposited and adsorbed metals
5. Particles and particulates
6. Impurities absorbed or entrapped by oxides.

Second, the methods of vapor-phase cleaning can be classified into the following major categories and specific types of processes and techniques:

1. Physical interactions:
  - thermal and low-pressure techniques
  - sublimation
  - evaporation and volatilization
  - argon ion oxide sputter etching
2. Physically-enhanced chemical reactions:
  - reactive ion bombardment
  - glow discharge plasma reactions
  - remote RF and microwave discharge hydrogen plasma reactions
  - electron cyclotron resonance hydrogen plasma reactions
  - ultraviolet-ozone-atomic oxygen organics oxidation
  - photochemically-enhanced metal reactions
  - ultraviolet-activated halogen metal reactions
3. Chemical thermal reactions:
  - thermal oxide decomposition in vacuum
  - volatile metal organics formation
  - anhydrous HF gas-phase oxide etching
  - wet HF vapor-phase oxide etching
  - HF-alcohols vapor-phase oxide etching
4. Mechanical techniques:
  - high-velocity dry-ice ( $\text{CO}_2$ ) jet scrubbing
  - cryogenic argon-aerosol jet impingement
  - pulsed laser radiation particle dislodgment
  - supercritical/subcritical fluid ( $\text{CO}_2$ ) pressure cycling

**Removal of Contaminants by Vapor-Phase Cleaning Methods.**

The methods and techniques listed in the preceding section are not just hypothetical possibilities. Specific examples can be cited that demonstrate their practical feasibility and implementation (see Sec. 4.0). The summary below indicates in general terms which of these methods is most appropriate for removing the various types of contaminants from semiconductor wafer surfaces.

Organic contaminants can be removed, depending on their composition, by one of the following methods: volatilization in vacuum at elevated temperature, oxidative degradation by the UV/O<sub>3</sub> reaction, remote or downstream oxygen plasma treatment, and plasma glow discharge reactions. These methods are applicable to all types of semiconductor wafers.

Native and chemical thin films of oxides and silicate glasses require chemical etching or physical sputter etching for their removal. The latter can lead to erosion of the semiconductor surface. Techniques for gas-phase etching with anhydrous HF, or vapor-phase etching with HF-H<sub>2</sub>O, have been well established (see Ch. 7). Alternative techniques for oxide removal are reduction annealing in H<sub>2</sub> under UHV (ultra-high vacuum) conditions at high temperature, low-energy ECR plasma etching in Ar or with NF<sub>3</sub>, thermal desorption at high temperature in vacuum or by plasma enhancement for pre-epitaxial cleaning of silicon wafers, and remote hydrogen plasma techniques.

Physisorbed and chemisorbed ions and deposited elemental metals require chemical processes to remove them from the semiconductor or oxide surfaces. Techniques of physical enhancement are frequently used to decrease the thermal energy requirement by supplying electromagnetic radiation or energy from plasma environments. However, these activated chemical reactions can have adverse radiation effects and cause ion-induced damage of the substrates. Typical examples are the removal of metallic impurities by remote microwave plasma or by photo-induced reactions, such as UV-generated chlorine radicals. Strictly chemical approaches are based on the formation of volatilizable species, such as metal chelates or nitrosyl compounds. The key requirement for removing chemical impurities is the formation of volatilizable species by reaction at low temperature, followed by their elimination at an elevated temperature and at low pressure.

Special attention must be paid to the state in which contaminants occur. Elemental metals and other impurities are often present as absorbates or inclusions in the native oxide film rather than being exposed in pure form

on the semiconductor surface. Etching in HF gas may be necessary to first remove the oxide cover and make the impurities accessible for chemical reactions.

The removal of particles and particulates in the gas or vapor phase from wafer surfaces is another difficult problem. Chemical reactions as described could be used to transform them into some volatile species, depending on their composition and size. Vapor etching of an oxide film on which particles are located or in which they are imbedded could be effective if the wafers are positioned vertically and if a vigorous flow of inert gas would sweep the freed particles away from the wafer.

The mechanical gas-phase techniques listed above have shown promise for the removal of both inert and reactive particles, but there may be problems of substrate damage and technical implementation that must be overcome.

### **4.0 EVOLUTION OF WAFER CLEANING SCIENCE AND TECHNOLOGY**

In this section we will trace the evolution of semiconductor wafer cleaning science and technology from the beginning; that is, from the advent of semiconductor device fabrication, to the present time. Four periods of this development can be discerned: *(i)* the early days from 1950 to 1960; *(ii)* the development period of wet-chemical cleans from 1961 to 1971; *(iii)* the widespread evaluation, application, and refinement of wet cleans from 1972 to September 1989, and finally *(iv)* the era of explosive research and development activity in both wet and dry cleaning methods from October 1989 to mid-1992.

The introduction section of each chapter in this book usually includes historical remarks pertaining to the chapter topic. The present systematic overall survey of the entire field should serve in establishing a comprehensive perspective of this evolution.

#### **4.1 Period from 1950 to 1960**

Harmful effects of impurities on the performance of simple transistors were recognized already in the early days of germanium devices; these problems became more apparent with the advent of silicon transistor fabrication in the later 1950s. Some sort of wafer cleaning was deemed necessary as part of the device manufacturing process.

Early cleaning techniques consisted of mechanical and chemical treatments. Particulate impurities were removed by ultrasonic treatment in detergent solutions or by brush scrubbing. The first caused frequent wafer breakage and the second often deposited more debris from the bristles than it removed from the wafer surfaces. Organic solvents were used to dissolve wax residues and other gross organic impurities.

Chemical treatments consisted of immersion of the wafers in aqua regia, concentrated hydrofluoric acid, boiling nitric acid, and hot acid mixtures as cleaning chemicals. Mixtures of sulfuric-acid/chromic-acid led to chromium contamination and caused ecological problems of disposal. Mixtures of sulfuric acid and hydrogen peroxide caused sulfur contamination. Nitric acid and hydrofluoric acid were impure and led to redeposition of impurities. In general, impurity levels and particles in process chemicals were high and in themselves tended to lead to surface contamination.

Aqueous solutions containing hydrogen peroxide had long been used for cleaning electron tube components (86)(87), but had never been investigated for possible applications to semiconductor wafer cleaning.

Plasma ashing was the first dry process applied to wafer cleaning for removing organic photoresist patterns, but left high concentrations of metallic compounds and other inorganic impurity residues.

#### **4.2 Period from 1961 to 1971**

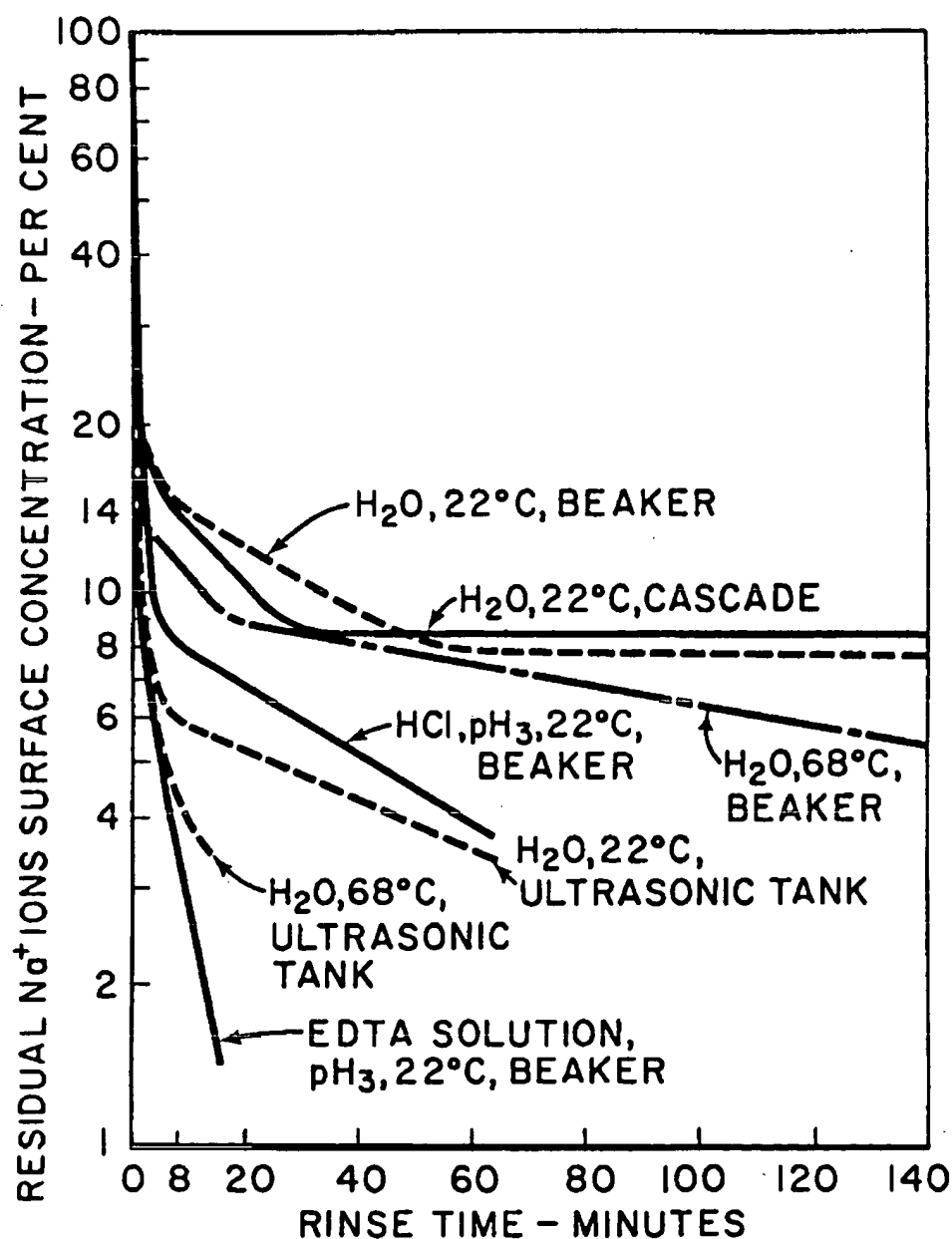
This period can be considered one of research into semiconductor surface contamination and the systematic development of wafer cleaning procedures.

**Radiochemical Contamination Studies.** Radioactive isotopes offered a unique opportunity for the study of surface contamination with an unprecedented degree of sensitivity. Although it had been applied to several other areas of semiconductor research, very few papers had been published prior to 1963 on the use of radioactive tracers for surface contamination studies, notably papers by Wolsky et al. for germanium (88), Sotnikov and Belanovskii for silicon (89), and Larrabee for GaAs and InSb (90).

In a series of intensive contamination studies, Kern applied radioactive tracer methods to investigate the concentrations of contaminant elements that were transferred onto electronic materials during manufacturing operations. It may be of interest to look at some of these still useful early results, which were published in 1963 (91)(92).

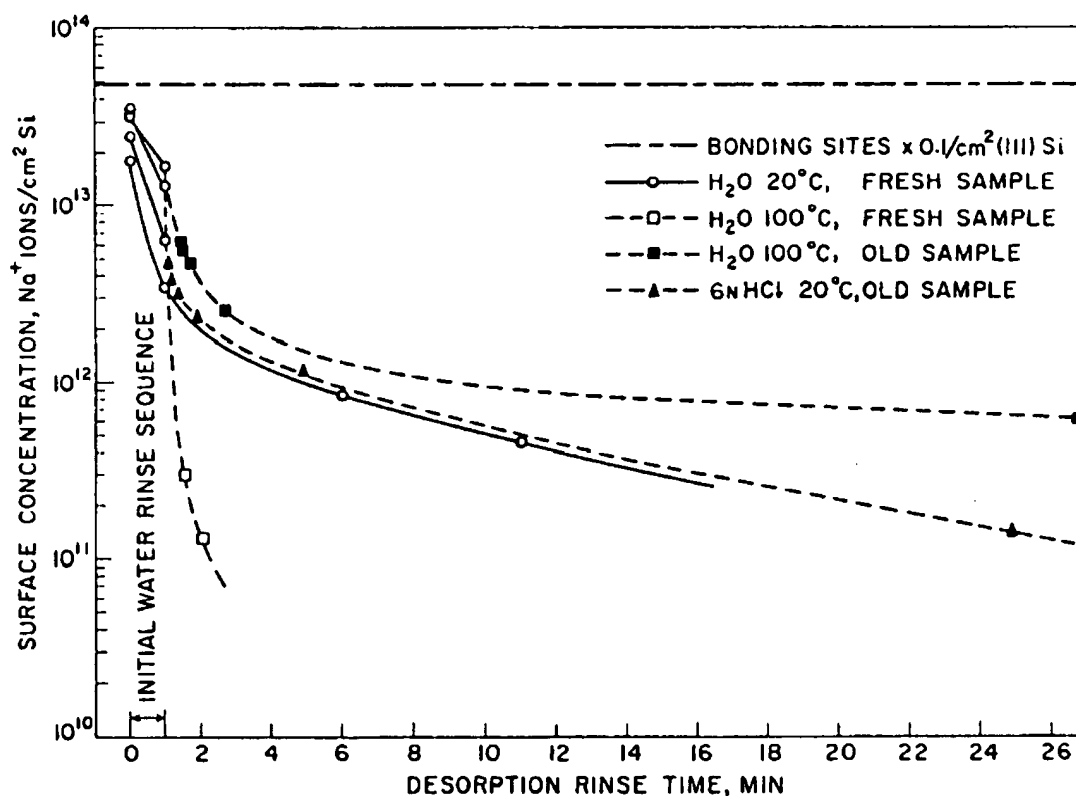
The adsorption of sodium ions on the assembly parts of germanium transistors (RCA 2N217, pnp) during the germanium anodic etching step in

alkali electrolyte solution was investigated with sodium-22 radioactive tracer. The desorption of sodium ions was tested after preliminary water rinses. The efficiency of various treatments was then assessed by measuring the radioactivity as a function of treatment time. Germanium pellets that has been cascade-rinsed with DI water had a concentration of  $6.2 \times 10^{14}$  sodium ions per  $\text{cm}^2$ . The plots in Fig. 1 demonstrate several interesting results. For example, EDTA chelating solution (as the free acid) was 280 times more effective than counter-current cascade rinsing with cold DI water.



**Figure 1.** Efficiencies of various desorption treatments for removing sodium ions from germanium transistors electrolytically etched in radioactive  $\text{Na}^{22}\text{OH}$  solution (90)(91).

A similar investigation was conducted with the components of a silicon power transistor (RCA 2N1482, npn). In this work, sodium-24, the isotope of sodium with a half-life of 15 hours, was created by neutron activation to attain several thousand times greater radioactivity levels than were available for the work with the germanium transistors, so as to achieve a much greater analytical sensitivity. Etching of various transistor parts in this highly radioactive NaOH solution and preliminary rinsing were performed entirely by remote-control manipulation in a radiation hot-cell. The efficiencies of several different treatments for desorbing sodium ions from various transistor parts were then determined by measuring the radiation intensity. The final concentration on silicon wafers after a dip in HCl solution and rinsing in DI water was  $<8 \times 10^{11} \text{ Na}^+/\text{cm}^2$ .



**Figure 2.** Inhibition effects of aging on desorption of  $\text{Na}^+$  ions from silicon wafers with DI  $\text{H}_2\text{O}$  and 6N (19%) HCl. Wafers were immersed in 0.025N  $\text{Na}^{22}\text{OH}$  followed immediately by initial rinsing for 60 sec. Subsequent desorption treatments within 24 hrs (*open symbols*) are compared with those after several weeks of storage (*solid symbols*) (93 I).

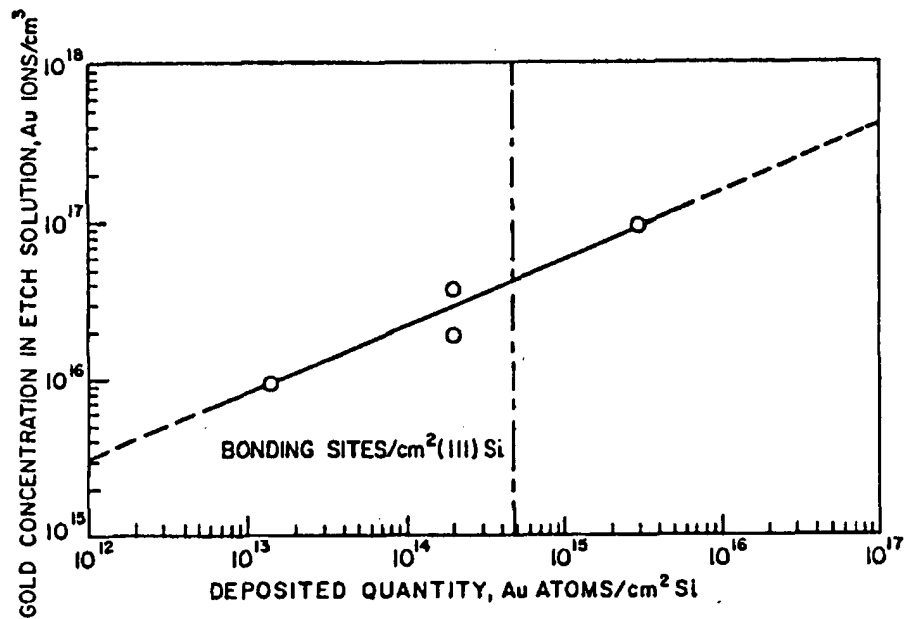


Contamination of silicon transistors by metallic impurities from solutions was assessed by use of the radioactive isotopes chromium-51, iron-59, copper-64, and gold-198. Techniques were devised to minimize residual concentrations, leading to a product yield increase for a silicon power transistor type (RCA 2N2102) of over two hundred percent in production.

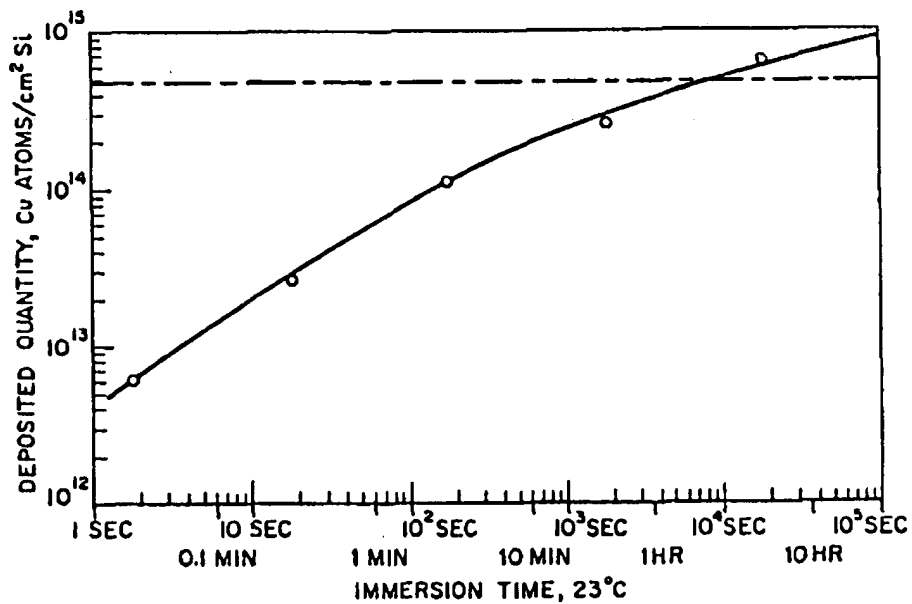
The contamination of silicon, germanium, and gallium arsenide wafers during wet-chemical etching and processing was also investigated with radiotracers. Known quantities of radioactively tagged trace metals were added to the processing liquids used for treating the wafers. The spatial distribution of residual metals after rinsing with DI water was examined by autoradiographic film techniques. The surface concentrations were determined by correlation with radiation intensity measurements. The effectiveness of various rinsing and cleaning treatments was also measured quantitatively.

The adsorption of constituents of etchant solutions on semiconductor wafers was investigated by use of the appropriate radionuclides: sodium-22 and -24 for NaOH, fluorine-18 for HF-containing etchants, chlorine-38 for HCl, iodine-131 for polishing etchants containing iodine, and carbon-14 labeled acetic acid for isotopic etchants containing this chemical. Analytical techniques similar to those described for trace contaminants in solutions were applied to measure adsorption and desorption phenomena.

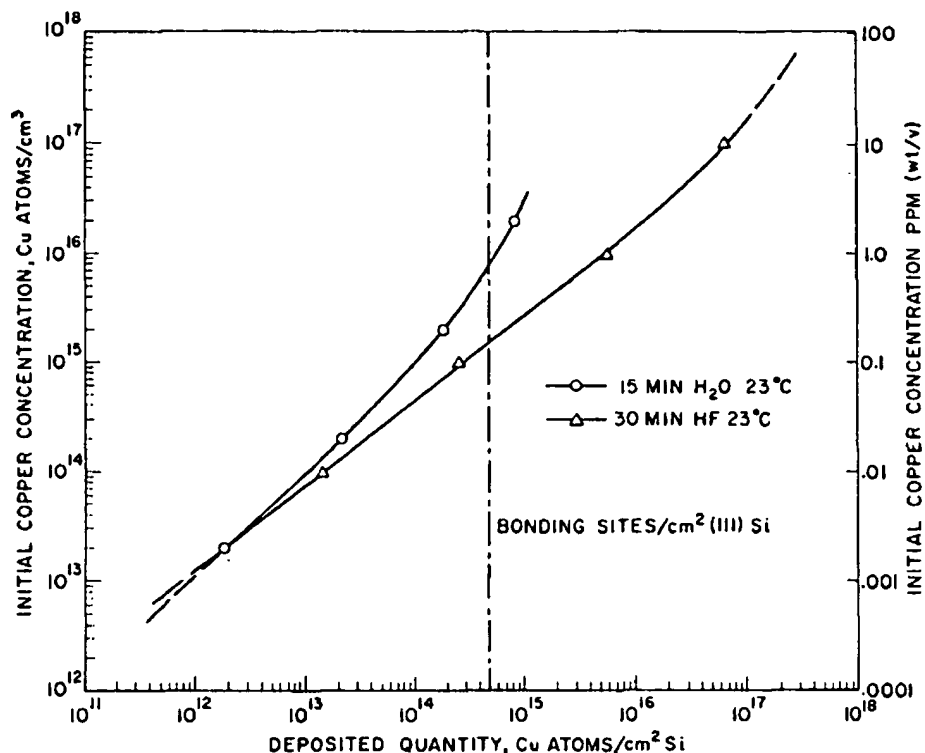
These radioactive tracer investigations were later extended to include additional metallic contaminants, substrates etchants, solutions, and cleaning agents. The radionuclides used as contaminant tracers included  $\text{Mn}^{54}$ ,  $\text{Zn}^{65}$ ,  $\text{Mo}^{99}$ ,  $\text{Sb}^{122}$ , and  $\text{Sb}^{124}$  in addition to the previously used metal tracers  $\text{Cr}^{51}$ ,  $\text{Fe}^{59}$ ,  $\text{Cu}^{64}$ , and  $\text{Au}^{198}$ , and the reagent component tracers  $\text{C}^{14}$ ,  $\text{F}^{18}$ ,  $\text{Na}^{22}$ ,  $\text{Na}^{24}$ ,  $\text{Cl}^{38}$ , and  $\text{I}^{131}$ . Discs of fused quartz were used as substrates in addition to Si, Ge, and GaAs wafers. Contaminant adsorption was measured for many typical etchants and reagents containing the radioactively marked ions, and their desorption was investigated for many reagents, chelating agents, and cleaning solutions. For example, acidic  $\text{H}_2\text{O}_2$  solutions were most effective for desorbing Au, Cu, and Cr from Si and Ge; HCl for Fe on Si; EDTA and other chelates suppressed deposition of Cu on Ge from solutions by  $10^2$  to  $10^3$ . The results for silicon and quartz were reported in three extensive papers published in 1970 (64)(93 I)(93 II); the work with germanium and gallium arsenide was published in 1971 (93 III). A few typical metal desorption data plots of current interest are reproduced in Figs. 3 - 8 for silicon and in Fig. 9 for gallium arsenide.



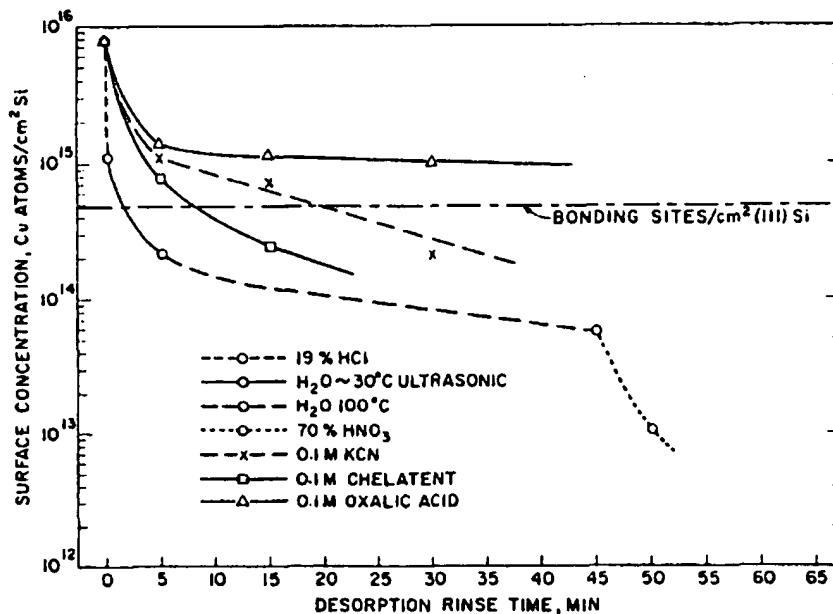
**Figure 3.** Numbers of gold atoms deposited on silicon wafers from etchant as a function of gold ions in solution.  $\text{Au}^{198}$  was added as a radioactive tracer to the  $\text{HF-HNO}_3\text{-CH}_3\text{CO}_2\text{H-I}_2$  etchant. Vertical dashes indicate number of bonding sites on (111)-Si (as a reference only) (93 II).



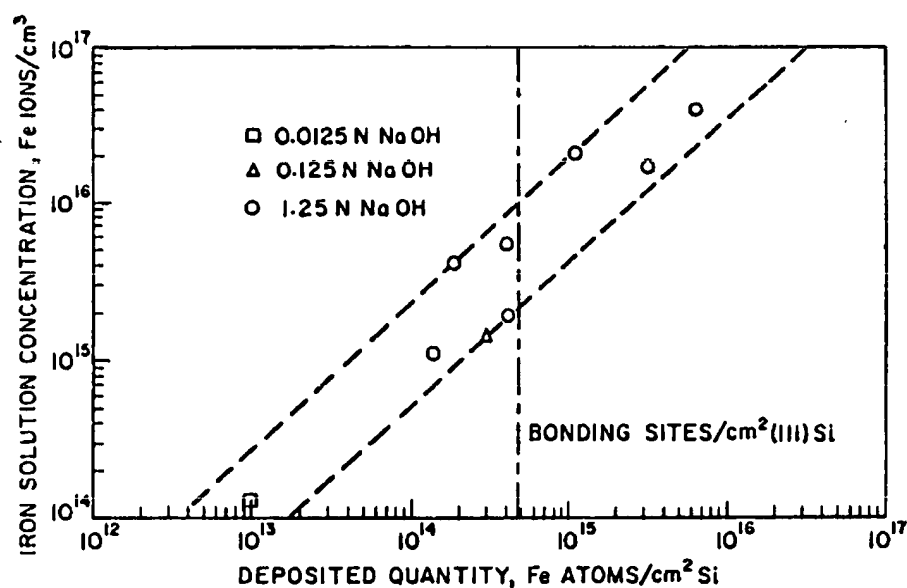
**Figure 4.** Number of copper atoms deposited on silicon wafers from 49% HF solution as a function of immersion time at 23°C. The acid contained 0.1 ppm copper tagged with  $\text{Cu}^{64}$  (93 II).



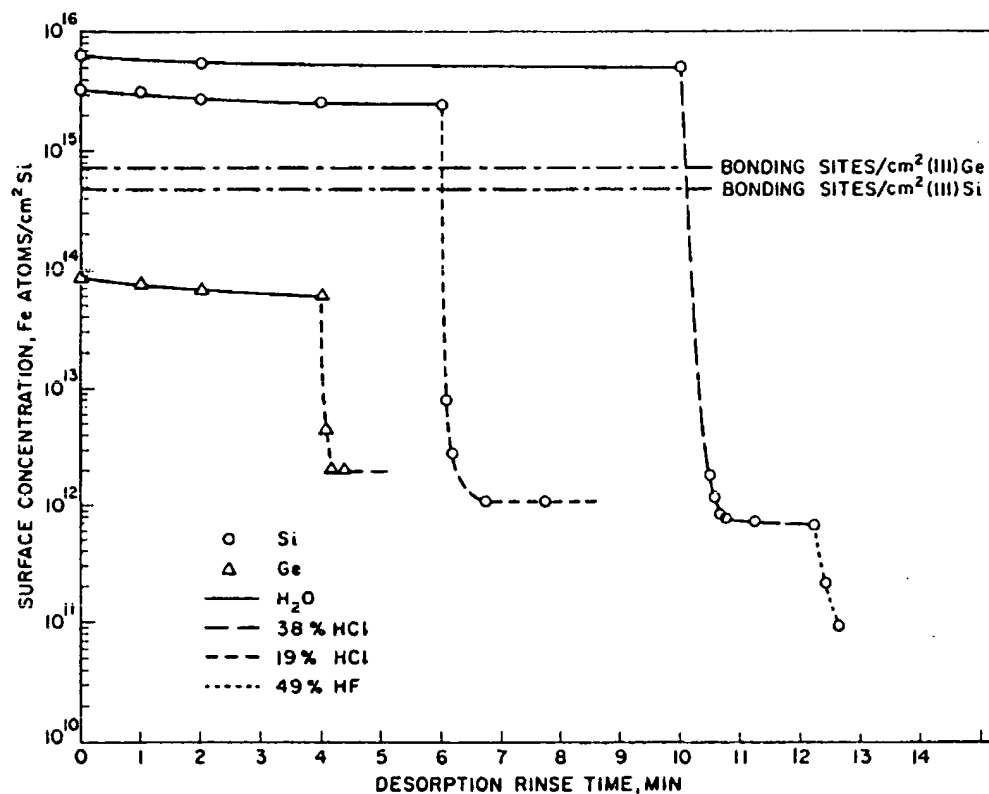
**Figure 5.** Quantity of copper deposited on silicon wafers from 49% HF solution and DI-distilled water as a function of copper concentration in solution.  $\text{Cu}^{64}$  was used as the radioactive tracer. Prior to immersion in the radioactive water the wafers had been dipped in non-radioactive HF and rinsed in non-radioactive water (93 II).



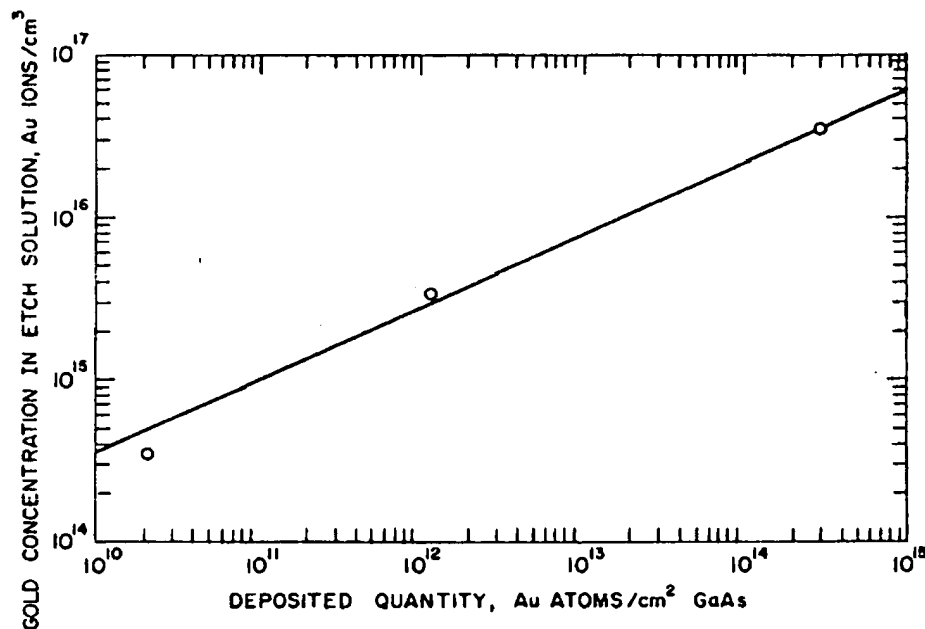
**Figure 6.** Effectiveness of various cleaning agents for desorbing heavy copper deposits from hot 5% NaOH solution with  $\text{Cu}^{64}$ -labeled Cu. Desorbing treatments were conducted at 23°C except for water rinses. Chelating agent is pentasodium diethylenetriamine pentacetate (93 II).



**Figure 7.** Quantity of iron deposited on silicon wafers from NaOH solutions as a function of iron solution concentration. Fe<sup>59</sup> was used as the radioactive tracer in NaOH solutions of the concentrations indicated. Wafers were immersed at 100°C for 1 min (93 II).

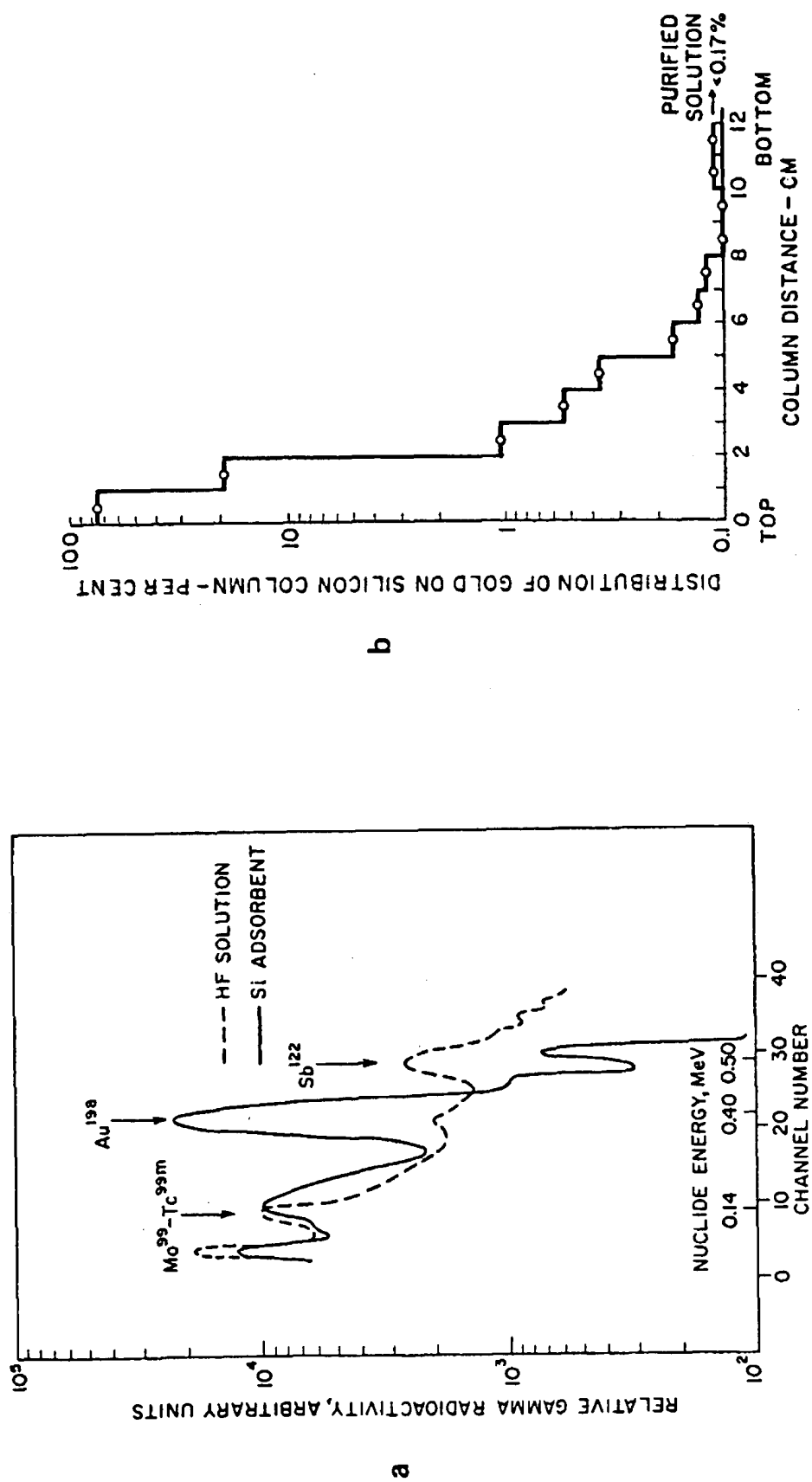


**Figure 8.** Efficiency of water and acid solutions at 23°C for desorbing iron adsorbates from silicon and germanium wafers. Fe<sup>59</sup>-containing deposits from hot NaOH were used. Number of bonding sites for Si and Ge are indicated for reference (93 II).



**Figure 9.** Number of gold atoms deposited on (100)-GaAs wafers from etchant as a function of gold ions in solution. A polishing etchant of 5 vol  $\text{H}_2\text{SO}_4$  (98%) - 1 vol  $\text{H}_2\text{O}_2$  (30%) - 1 vol  $\text{H}_2\text{O}$  containing  $\text{Au}^{198}$  as radioactive tracer was used. Each data point is the average of radioactivity measurements from three wafers (93 III).

The strong concentrating efficiency of silicon for gold from HF solution is shown in Fig. 10a, and its possible utilization for purifying HF solution is demonstrated in Fig. 10b. The dashed gamma radiation spectrum in Fig. 10a shows that of a 1N HF solution containing antimony-122, molybdenum-99 with its associated technetium-99, and gold-198 showing as a minor peak. The solid curve, obtained from silicon wafers that had been immersed in this solution, was normalized with the  $\text{TC}^{99\text{m}}$  peak maximum of the solution spectrum. The extremely high degree of selective deposition of metallic gold on the silicon is dramatically evident by comparing the  $\text{Au}^{198}$  peak intensities. The utilization of this effect is exemplified in Fig 10b: percolating a 49% HF solution containing  $\text{Au}^{198}$  through a column of high-purity silicon crystal pieces resulted in a retention of more than 95% of the gold in the first sixth of the column, and more than 98.8% removal in a single pass. Similar results were obtained with copper and other heavy metals in HF, BHF, and  $\text{H}_2\text{O}_2$  solutions.



**Figure 10.** (a) Gamma radiation spectra of an HF solution and its adsorbate on silicon, demonstrating the strong accumulation efficiency of gold on silicon (93 II). (b) Distribution of radioactively marked gold from 49% HF solution on a chromatographic column of silicon crystal particles (91).

An unconventional approach to contaminant transfer measurements by radiochemical techniques should be mentioned before we leave this topic. This study, which had also been conducted and published by the author (95), concerned the transfer of impurity elements from crucibles. In this study the crucibles were radioactivated by bombardment with thermal neutrons in a nuclear reactor to produce radionuclides from the quartz impurity elements and the silicon. The GaAs crystals were then synthesized in these highly radioactive crucibles. Gamma ray scintillation spectrometry of the ingot sections allowed identification and quantitative measurements of the transferred contaminants. The results led to improved processing techniques for the crystal growth synthesis of GaAs.

**Development of the Original RCA Wafer Cleaning Procedure.** In this section we present a brief commentary on the development of the original RCA standard cleans by Kern and Puotinen, as published in 1970 (64).

The development of an optimized wet-cleaning procedure for silicon wafers proceeded concurrently with the contamination studies described in the previous section, which provided important information on adsorption and desorption characteristics of many contaminants.

It was realized early on that the first step should remove organic contaminants to expose the silicon surface; some kind of wet oxidant was needed to achieve this. Adsorbed ions and metals would then have to be removed by some solubilizing oxidant reagent. To prevent redeposition of the dissolved ionic contaminants, some complexing agent would be required. In addition, a set of important technological considerations, listed in Table 10, would have to be fulfilled in formulating an ideal procedure.

Thermodynamic reasoning based on the oxidation potentials of several possible candidates were an important consideration in reactant selection. Figure 11, reproduced from the original paper in 1970, shows the oxidation potentials for several common reactions as a function of pH; note that oxidizing power increases with decreasing (more negative) electrode potential. For equivalent concentrations, the peroxide oxidation reaction is the most powerful oxidizing agent shown. The selection of hydrogen peroxide as the primary reagent in the procedure was, therefore, the obvious choice, especially since it also met the criteria in Table 10 and had been used in cleaning mixtures for electron tube components. The reactive additives selected were ammonium hydroxide for the first solution and hydrochloric acid for the second. Both chemicals have the desired chemical reactivity, are volatile, are compatible with the criteria in Table 10, and were

readily accessible in relatively pure form like the hydrogen peroxide. Salient features are summarized in Tables 11 and 12, which we presented in Sec. 3.3.

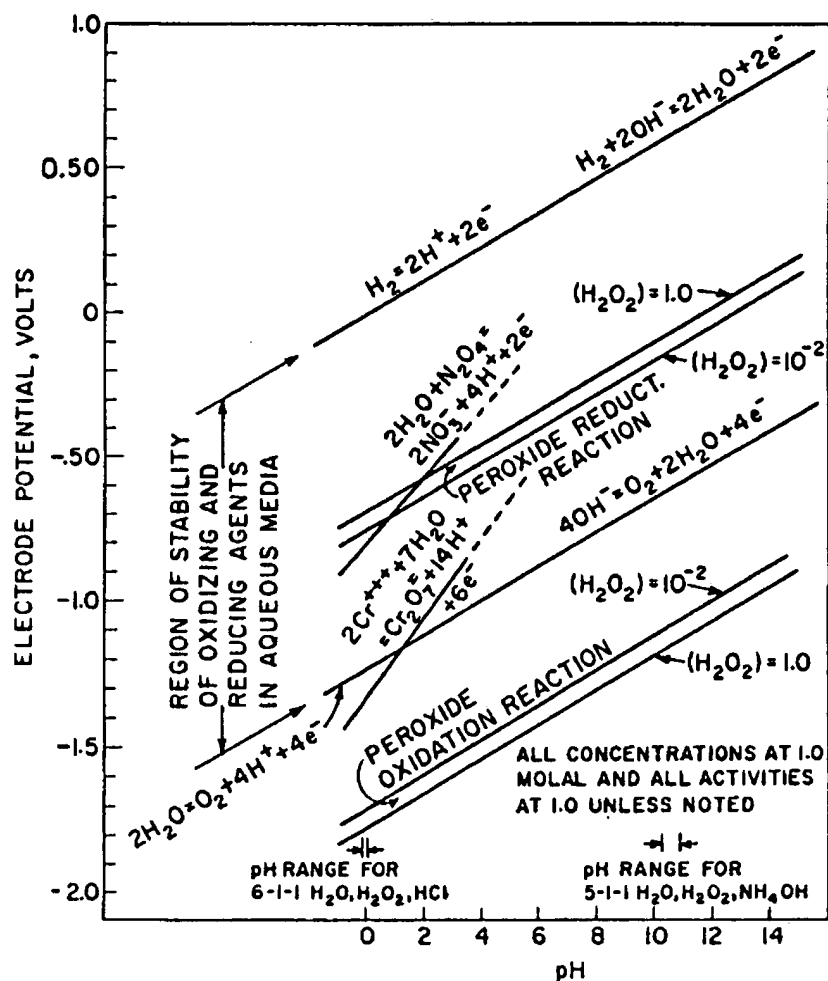


Figure 11. Electrode potentials vs. pH for various redox systems at 25°C (64).

The first solution (SC-1) was designed to remove organic surface impurities by the solvating action of the  $NH_4OH$  and the powerful oxidation capability of the  $H_2O_2$ . It was realized that the  $NH_4OH$  would also serve as a complexant for many metallic contaminants; copper, for example, forms the  $Cu(NH_3)_4^{+2}$  amino-complex.

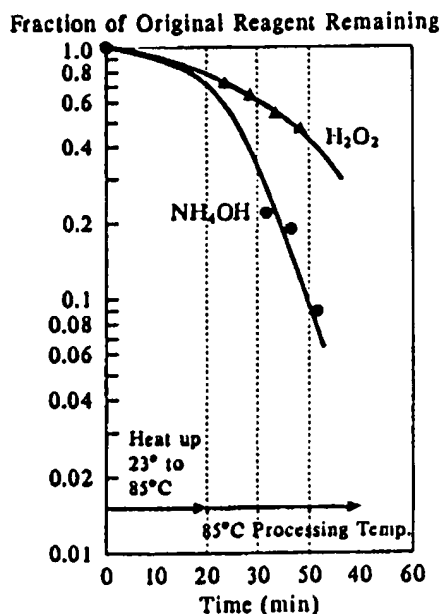
The volume ratios for  $H_2O-H_2O_2-NH_4OH$  that were recommended originally are in the range of 5:1:1 to 7:2:1 (or 5:1.4:0.7). Most people have used the 5:1:1 ratio since there seemed to be no obvious difference within this range.



The second solution (SC-2) was formulated to remove residual heavy-metals and prevent electrochemical displacement replating from solution by forming soluble complexes with the resulting ions. This strongly acidic mixture also dissolves alkali ions and metal hydroxides. The volume ratios recommended for  $\text{H}_2\text{O}$ - $\text{H}_2\text{O}_2$ - $\text{HCl}$  ranged from 6:1:1 to 8:2:1 (or 6:1.5:0.75). The first ratio has been used most often; sometimes the same ratio as for SC-1 (5:1:1) is used for simplicity, without adverse effects.

The volume ratios and processing conditions were determined empirically by performance tests. The originally-used conditions were 10 - 20 min at 75 - 85°C (these were later reduced to 10 min at 75 - 80°C, and finally to 10 min at 70°C, to minimize etching effects and the decomposition rate of the  $\text{H}_2\text{O}_2$ ). Additional details have been given in Sec. 3.3.

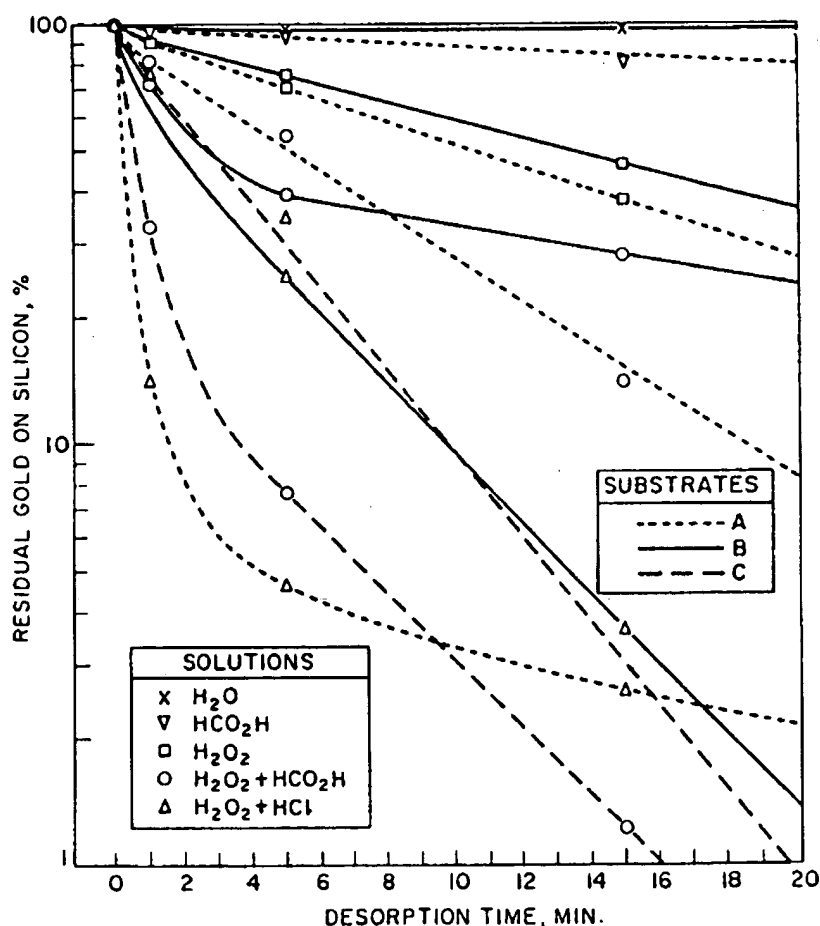
The cleaning procedure was carried out by simple immersion of the wafer batches in quartz carriers into SC-1 and SC-2 baths. Vessels of fused quartz were specified to prevent leaching of aluminum, boron, and alkalis from glass if Pyrex had been used. A condenser minimizes volatilization of  $\text{NH}_3$  from SC-1 and  $\text{HCl}$  from SC-2. The graph in Fig. 12 shows the worst-case situation (open vessel, excessively high temperature, long use time) for the critical SC-1 mixture in which the  $\text{H}_2\text{O}_2$  decomposes much more rapidly than in the acidic SC-2. We recommended that the reactions be terminated by overflow quenching with cold DI water before transferring the wafer batches to a flow rinse station with ultra-filtered DI water.



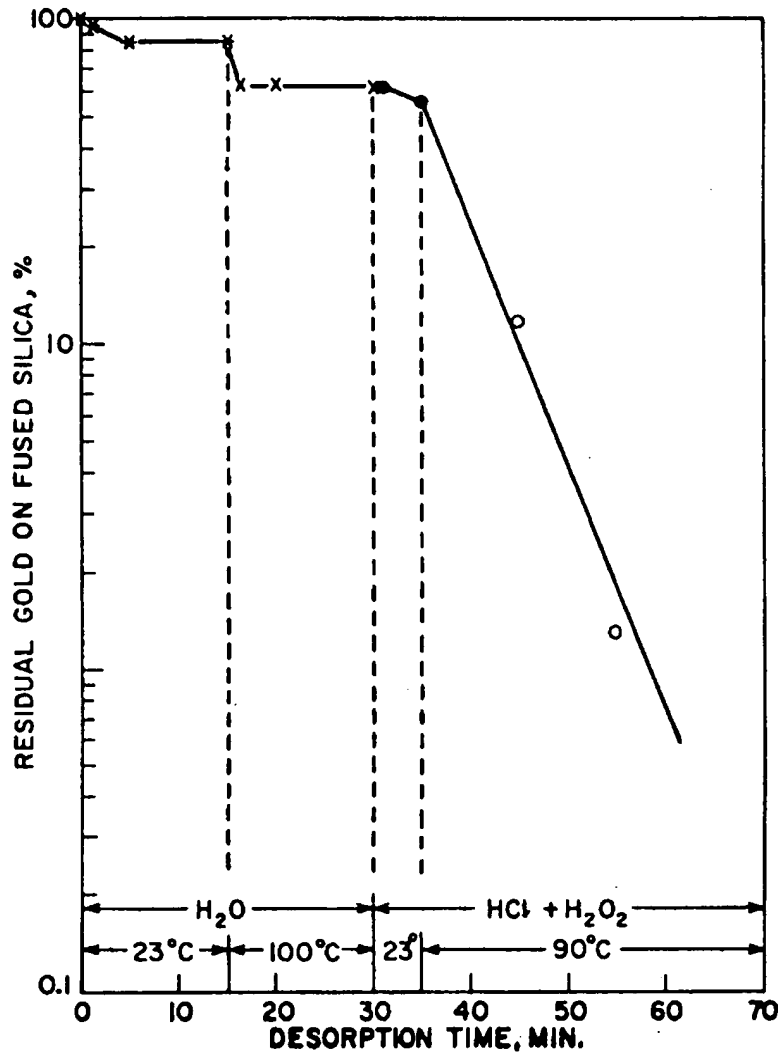
**Figure 12.** Decrease of the  $\text{H}_2\text{O}_2$  and  $\text{NH}_4\text{OH}$  concentration in 5:1:1 SC-1 as a function of use time at excessively high temperature and long time periods in an open container. The decomposing  $\text{H}_2\text{O}_2$  emits  $\text{O}_2$ , and the  $\text{NH}_4\text{OH}$  gives off  $\text{NH}_3$ . (After Ref. 62.)

Stripping of the native or chemically formed hydrous oxide films before and after SC-1 with very dilute (1:50 - 1:100) HF-H<sub>2</sub>O was also investigated but considered optional because no conclusive experimental results were available to clearly justify its use. These aspects are further discussed in Sec. 3.3.

The effectiveness of the RCA cleaning procedure for silicon wafers, as described in the original publication (64), had been assessed with sensitive water spray wetting tests for organic contaminants, capacitance-voltage bias-temperature measurements on metal-oxide-semiconductor capacitors for ionic contaminants, and radioactive tracer analysis for metal desorption, as shown in the reproduced Figs. 13 - 15.

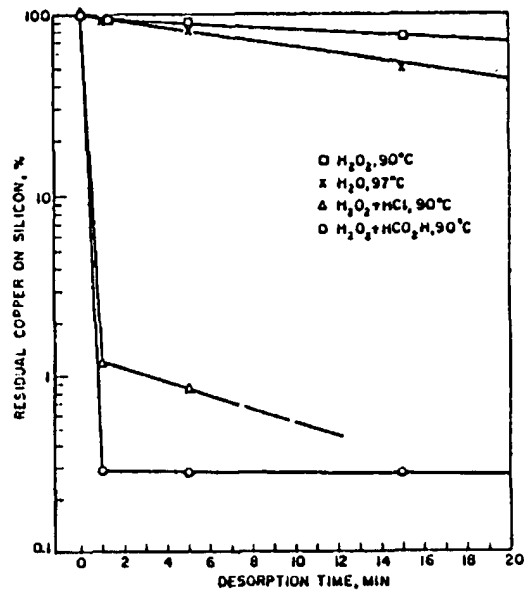


**Figure 13.** Efficiency of various cleaning agents at 90°C for desorbing heavy gold deposits from silicon. The wafers were etched in Au<sup>198</sup>-containing solutions and had the following surface concentrations (Au/cm<sup>2</sup>): curve A (dotted):  $7 \times 10^{13}$ , from HNO<sub>3</sub>-HF, curve B (solid):  $2 \times 10^{15}$ , from HF, curve C (dashed):  $3 \times 10^{15}$ , from HF-HNO<sub>3</sub>-I<sub>2</sub>-CH<sub>3</sub>CO<sub>2</sub>H. Desorption solutions: x = DI-distilled H<sub>2</sub>O, ∇ = H<sub>2</sub>O-HCO<sub>2</sub>H (90%) (9:1), □ = H<sub>2</sub>O-H<sub>2</sub>O<sub>2</sub> (30%) (9:1), ○ = H<sub>2</sub>O-H<sub>2</sub>O<sub>2</sub>-HCO<sub>2</sub>H (8:1:1), Δ = H<sub>2</sub>O-H<sub>2</sub>O<sub>2</sub>-HCl (1N) (8:1:1) (64).

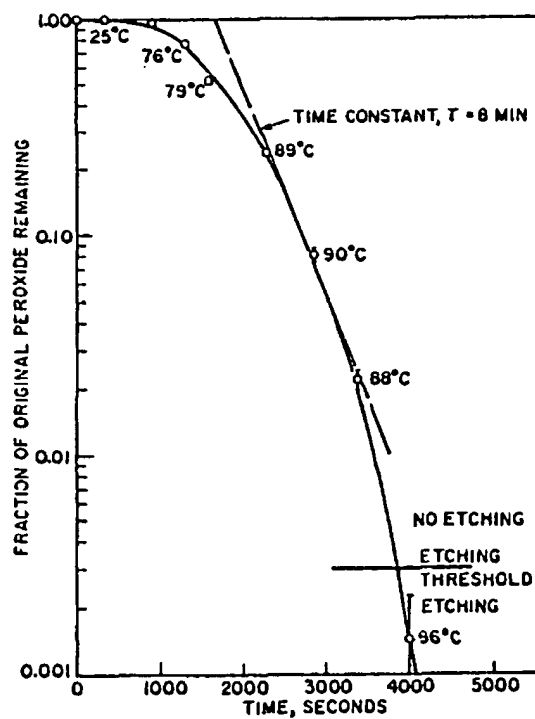


**Figure 14.** Desorption efficiency for gold (marked with  $\text{Au}^{198}$ ) from fused quartz surfaces under various conditions. Quartz plates were etched in 49% HF containing  $\text{Au}^{198}$ ; 100% =  $1.6 \times 10^{12}$  Au atoms/cm<sup>2</sup>. The HCl +  $\text{H}_2\text{O}_2$  mixture consisted of 8 vol  $\text{H}_2\text{O}$  - 1 vol diluted HCl (1N) - 1 vol  $\text{H}_2\text{O}_2$  (30%) (64).

Silicon etching effects for various solution compositions and the addition of fluoride were also studied. No silicon etching of the 5:1:1 SC-1 solution at that time could be observed even if substantially lower  $\text{H}_2\text{O}_2$  concentrations were used. These results demonstrated a wide margin of process safety when used in the fab (see Fig. 16).



**Figure 15.** Desorption efficiency of various agents for removing  $\text{Cu}^{64}$ -labeled heavy copper deposits from silicon wafers. The initial Cu concentration from HF solution was five times higher for the  $\text{H}_2\text{O}_2$  - HCl test than for the others (64).



**Figure 16.** Silicon etching threshold and fraction of  $\text{H}_2\text{O}_2$  remaining for 5:1:1 SC-1 solution as a function of use time at high temperature. The approximate etching threshold for (111)- and (100)-Si is indicated by the horizontal bar (64).

### 4.3 Period from 1972 to 1989

**Chronological Survey of the Literature on  $\text{H}_2\text{O}_2$ -based Cleans\*.** Beginning in 1972, independent investigators examined and verified by various analytical methods the effectiveness of the RCA cleaning method published in 1970 (64). In this section we review chronologically references on silicon wafer cleaning pertaining primarily to hydrogen peroxide solutions. The period covered extends from 1972 up to the First International Symposium on Cleaning Technology in Semiconductor Device Manufacturing in October 1989 (1).

In 1972, Henderson published results of the evaluation of SC-1/SC-2 cleaning, using high-energy electron diffraction and Auger electron spectroscopy as analytical methods (96). He concluded that the process is well suited for wafer cleaning prior to high-temperature treatments, as long as quartzware is used for processing, as specified by us (64). An additional final etch in HF solution after SC-1/SC-2 caused carbon contamination and surface roughening during vacuum heating at  $1100^\circ\text{C}$  due to loss of the protective 1.5 nm thick C-free oxide film remaining after SC-2. Meek et al. (1973) investigated the removal of inorganic contaminants, including Cu and heavy metals, from silica-sol polished wafers by several reagent solutions (97). Using Rutherford backscattering, they concluded that SC-1/SC-2 pre-oxidation cleaning removes all elements heavier than Cl. Sulfur and chlorine remained after either SC-1, SC-2, or other cleaning procedures at  $10^{13}/\text{cm}^2$ . SC-1/SC-2 cleaning eliminated Ca and Cu much more reliably than did HF- $\text{HNO}_3$ .

Amick (1976) reported the presence of Cl on Si after SC-2 and S after  $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$ ; he used spark-source mass spectrometric analysis (98). In 1976 Kern and Deckert published a brief review of surface contamination and semiconductor cleaning as part of a book chapter on etching (58). Murarka et al. (1977) studied methods for oxidizing Si without generating stacking faults and concluded that SC-1/SC-2 prior to oxidation is essential for this purpose (99). Gluck (1978) discussed removal of gold from Si by a variety of solutions. The desorption efficiency of SC-1 was more effective than that of SC-2, but the recommended sequential treatment of SC-1 followed by SC-2 was found the most effective method at high gold surface concentrations ( $10^{14}/\text{cm}^2$  range) (100).

Peters and Deckert (1979) investigated photoresist stripping by

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\* This section is reprinted by permission of the publisher; the paper was originally presented at the 1989 fall meeting of The Electrochemical Society, held in Hollywood, Florida (63).

solvents, chemical agents, and plasma ashing, The SC-1 procedure was the only acceptable technique by which the residues could be removed completely (101). Burkman (1981) reported on desorption of gold with several reagent solutions by centrifugal spraying. SC-1 type solution was much more effective than  $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$ , while a SC-2 type alone showed poor efficiency (74).

Phillips et al. (1983) applied SIMS (secondary ion mass spectroscopy) to determine the relative quantities of contaminants on Si. Cleaned wafers were purposely contaminated with gross quantities of numerous inorganic materials and then cleaned by immersion or spray techniques with various aggressive reagents, including aqua regia, hot fuming  $\text{HNO}_3$ , and  $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$ . The lowest residual concentrations for most impurity elements were obtained by spray cleaning with  $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$  followed by the SC-1/HF/SC-2 type cleaning sequence (102). Goodman et al. (1983) demonstrated by minority-carrier diffusion-length measurements the effectiveness of SC-1/SC-2 for desorbing trace metals on Si (103). The author (1983) published a review of the subject on the occasion of the Citation Classic declaration of the original 1970 paper (104).

In 1983 Watanabe et al. (105) reported dissolution rates of  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$  films in SC-1. The dissolution rate of thermally grown  $\text{SiO}_2$  in SC-1 during 20 min at  $80^\circ\text{C}$  was a constant 0.4 nm/min, a significant rate for structures with thin oxide layers. The etch rate of CVD  $\text{Si}_3\text{N}_4$  was 0.2 nm/min under the same conditions. Measurements by the author in 1981 (and published in 1984), however, indicated much lower oxide dissolution rates under nearly identical conditions (62). Film thicknesses were measured by ellipsometry after each of four consecutive treatments in fresh 5:1:1 SC-1 at  $85^\circ\text{C}$  and totaled only 7.0 nm/80 min, or 0.09 nm/min. Under the same conditions, 6:1:1 SC-2 showed no loss. Similar results averaging 0.13 nm/min were obtained with thermal  $\text{SiO}_2$  films grown on lightly or heavily doped Si. Wafers from the same sets were used to determine the etch rates of exposed Si in SC-1 solutions with decreasingly lower  $\text{H}_2\text{O}_2$  content. Little etching or attack of Si occurred (less than 0.8 nm/min), even when the  $\text{H}_2\text{O}_2$  concentration was reduced by 90% (62).

Bansal (1984, 1985) reported extensive results on particle removal from Si wafers by spray cleaning with SC-1/SC-2,  $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$ , and HF solutions of various purity grades. He found the RCA cleaning solutions the most effective (106)(107). Schwartzman et al. (1985) described simultaneous removal of particles and contaminant films by megasonic cleaning with SC-1 solutions (77). Ishizaka and Shiraki (1986) showed that atomi-

cally clean Si surfaces for MBE can be prepared below 800°C in UHV by thermal desorption (volatilization) of a thin (0.5 - 0.8 nm) passivating oxide layer that protects from carbon contamination (108). The layer was formed in a series of wet oxidation ( $\text{HNO}_3$ , SC-1) and HF-stripping steps, terminating with an SC-2 type treatment.

Wong and Klepner (1986) used XPS analysis to examine Si after wet chemical treatments. RCA cleaning without buffered HF stripping resulted in about 30% of the Si atoms in the top 1.0 nm being oxidized, whereas with a final BHF step, less than one monolayer of suboxide coverage resulted (109). Grundner and Jacob (1986) conducted extensive studies of Si surfaces after treatment with SC-1/SC-2 or 5% HF solutions, using x-ray photoelectron and high-resolution electron energy-loss spectroscopy. Oxidizing solutions produced hydrophilic surfaces, whereas HF solution led to hydrophobic surfaces consisting mainly of Si-H with some Si- $\text{CH}_x$  and Si-F (110).

In 1986 Becker et al. (111) reported on decontamination by different reagent sequences. SIMS analysis was used to test for the removal of Na, K, Ca, Mg, Cr, Cu, Al, and particle impurities. The best cleaning sequence for metallics was  $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2\text{/SC-1/HF/SC-2}$ . Reversing the order of SC-1 and HF was most effective for particle removal and slightly less so for metal ions. Kawado et al. (1986) found by SIMS that Al on Si wafers originated from impure  $\text{H}_2\text{O}_2$  used in SC-2. Very high concentrations resulted if Pyrex vessels were used in the processing instead of fused quartz (112). In 1986 McGillivray et al. (113) investigated effects of reagent contaminants on MOS capacitors. Low-field breakdown was more prevalent if pre-oxidation cleaning with SC-2 was terminated with HF solution instead of omitting it. No other significant differences in electrical properties resulted from these two treatments.

Lampert (1987) examined growth and properties of oxide films on Si in various aqueous solutions, including SC-1 and SC-2 (114). Gould and Irene (1987) studied the influence of pre-oxidation cleaning on Si oxidation kinetics (115). They found significant rate variations depending on treatment (SC-1/SC-2/HF, SC-1, SC-2, HF, no clean). Ruzyllo (1987) reported on similar experiments and found that various pre-oxidation cleans seem to affect structure and/or composition of the subsequently grown oxide rather than the reactivity of the Si surface (116). Slusser and MacDowell (1987) found that sub-ppm levels of Al in  $\text{H}_2\text{O}_2$  used for SC-1/SC-2 cause a substantial shift (up to 0.2 V) in the flat-band voltage levels of a dual dielectric. Aluminum concentrates on the wafer surface, and basic media

such as SC-1 lead to five times higher levels than acidic (SC-2) solutions (12). In 1987 Kern and Schnable reviewed wafer cleaning in a book chapter on wet-chemical etching (59).

Probst et al. (1988) stated that for achieving predictable diffusion from implanted doped poly-Si into single-crystal Si, an SC-1/SC-2 treatment of the substrate prior to poly-Si deposition is imperative (117). Khilnani (1988) discussed various aspects of semiconductor cleaning, including the RCA process (14). Peterson (1988) showed that the sequencing of cleaning solutions ( $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$ , SC-1, SC-2, HF) can have dramatic effects on particle levels (118).

In 1989 Morita et al. (119) reported on the contamination of SC-1/SC-2 cleaned wafers by Na, K, Al, Cr, Fe, Ni, and Cu from solutions, showing that the absence or presence of an  $\text{SiO}_x$  layer on the Si surface strongly affects adsorption. Desorption of Al and Fe was most effective with HF- $\text{H}_2\text{O}$ , and that of Cu and Cr with SC-2. The same authors (120) postulated that metals of high enthalpy of oxide formation adsorb on the oxidized Si surface by oxide formation, whereas metals of low ionization tendency deposit galvanically on the bare Si. Gould and Irene (1989) studied the etching of native  $\text{SiO}_x$  and Si in  $\text{NH}_4\text{OH-H}_2\text{O}$ , BHF, and SC-1 by ellipsometry. Severe Si surface roughness resulted from  $\text{NH}_4\text{OH}$ , less with BHF, and none with SC-1 (121).

Ohmi et al. (1989) compared particle removal efficiency of several cleaning solutions. They found that 5:1:1 SC-1 efficiently removes particles larger than  $0.5\text{ }\mu\text{m}$ , but increased those smaller than  $0.5\text{ }\mu\text{m}$  (haze) unless the  $\text{NH}_4\text{OH}$  ratio was decreased to one half or less, in which case both types of particles were reduced efficiently. However, no processing conditions and effects of low- $\text{NH}_4\text{OH}$  SC-1 on removal of chemical contaminant films were mentioned (78). Menon et al. (1989) evaluated effects of solution chemistry (5:1:1, SC-1, DI water) and particle composition on megasonic cleaning efficiency at various power levels. They concluded that cleaning efficiency depends on several factors and that megasonics can provide wafer cleanliness levels not previously attainable (72).

**Other Important Advances.** The previous section, being concerned with  $\text{H}_2\text{O}_2$ -based cleans, has not included other important developments that had taken place within the period of 1972 to September 1989. Since most of this work will be discussed in other chapters of this book, we will cover this topic in broad terms with only a few key references.

Significant advances in the science and technology of particles have led to a better understanding of the forces of adhesion, the nature of



submicron particles in liquids and gases, and the mechanisms of transfer to solid surfaces. Most of this work, such as that by Bowling (122), Mishima et al. (80) and Menon et al. (72)(123), was published between 1985 and 1989 and has resulted in improved high-purity processing and effective removal of particles from wafer surfaces, especially by the extended application of megasonic cleaning techniques.

Important advances were made in the area of dry cleaning of semiconductor wafers. The work by Vig (124), Kaneko et al. (125) and others extended the use of the UV/ozone method for removal of organic contaminants on silicon and III-V compound semiconductor surfaces. Mishima et al. (79)(80) and Ohmi et al. (78) conducted and published much research on wafer drying techniques, especially the subtleties of IPA vapor drying.

The introduction of anhydrous HF gas etching and HF-H<sub>2</sub>O vapor etching technology for removing oxide films on wafers to avoid particle contamination was pioneered by Claevelin, Duranko, and Novak (126), Clements et al. (127), and Duranko et al. (128). This major advance set the stage for the development of vapor-phase cleaning science and technology in general. Early investigations were conducted in remote plasma cleaning, an entirely different approach to dry cleaning, as exemplified by the work of Fountain et al. (129).

Another area associated with wafer cleaning where significant progress was made is the refinement of microanalytical chemical and instrumental methods for detecting and quantifying trace contaminants and for exploring the atomic structure and morphology of semiconductor surfaces. Much insight has been gained by elucidating the chemical surface reactions with HF reactants and silicon, for example, and the nature of the resulting passivated, hydrogenated silicon surface. Example references for papers on this subject are by Burrows et al. (130), Hahn et al. (131), Zazzera and Moulder (132), and Chabal et al. (133).

#### **4.4 Period of October 1989 to Mid-1992**

As already mentioned, this is the period of explosive growth in the field of wafer cleaning science and technology, and the rate of progress is still accelerating. Rather than attempting a comprehensive coverage of all results reported, which is beyond the scope of this chapter, we will consider highlights of the progress achieved in (i) wet-chemical cleaning processes and (ii) gas-phase cleaning methods, as they pertain to the removal of specific types of contaminants. Most of the information is contained in the voluminous literature (1)-(11) cited in the Introduction Sec. 1.2.

**Wet-Chemical Cleaning Processes.** New observations on the performance and effects of  $\text{H}_2\text{O}_2$ -based cleaning solutions have led to some modifications of the original RCA SC-1 cleaning procedure. In addition, high-purity chemicals have become available, including Al-free  $\text{H}_2\text{O}_2$ , low-particulate HF, and low-metal HCl and  $\text{NH}_4\text{OH}$  solutions that have led to much lower trace metal contamination levels from these sources than was previously possible.

Van den Meerakker and Van der Straaten (134) elucidated the mechanism of silicon etching inhibition by  $\text{H}_2\text{O}_2$  in SC-1 and studied the kinetics of etching. They reported a half-life for the standard 5:1:1 SC-1 of 16 min at  $70^\circ\text{C}$  and 9.3 min at  $80^\circ\text{C}$ . The authors stated that no etching occurs at  $70^\circ\text{C}$  as long as there is a  $\text{H}_2\text{O}_2$  concentration of at least  $3 \times 10^{-3}$  M present to passivate the silicon surface, which represents 0.2% of the  $\text{H}_2\text{O}_2$  concentration in the 5:1:1 SC-1. In other words, no etching was found as long as at least 1/500 of the original  $\text{H}_2\text{O}_2$  was present. The result agrees with the etching threshold of 0.4% indicated in Fig. 16 for a higher solution temperature (64).

Tanaka et al. (135) reported silicon etch rates for 5:1:1 SC-1 of 0.5 nm/min at  $75^\circ\text{C}$  and 0.8 nm/min at  $85^\circ\text{C}$ , with higher values for decreasing  $\text{H}_2\text{O}_2$  or increasing  $\text{NH}_4\text{OH}$  concentrations. These values are higher than those determined by the writer, which averaged 0.05 nm/min at  $80 - 85^\circ\text{C}$  (62). The discrepancy could be due to the long etch time used in the treatments by Tanaka et al. that could lead to a loss of the etch-protective oxide layer (134); variations in the silicon wafer properties could also be a cause (62). Although these etch rates are relatively low, it would be prudent not to exceed the SC-1 cleaning temperature of  $70^\circ\text{C}$  and the time of 10 min, as recommended in Sec. 3.3.

Microroughening of the silicon surface as a result of nonuniform microetching by 5:1:1 SC-1 solution has been investigated by many researchers, including Miyashita et al. (136), Ohmi et al. (137)(138), and Heyns et al. (139). This effect has become detectable on an atomic level only recently with the advent of atomic force microscopy. microroughening has detrimental consequences on the quality and breakdown voltage characteristics of thin, thermally grown gate oxide films, as reported by Meuris et al. (26), Verhaverbeke et al. (27)(31), Ohmi et al. (138), and Heyns et al. (139). Miyashita et al. (136) reported that a reduction of the  $\text{NH}_4\text{OH}$  concentration in the 5:1:1  $\text{H}_2\text{O}$ - $\text{H}_2\text{O}_2$ - $\text{NH}_4\text{OH}$  SC-1 mixture down to 5:1:0.1 to 5:1:0.01 not only eliminated the roughening but also enhanced\* the removal of particles. A reduction of the  $\text{NH}_4\text{OH}$  concentration to 5 - 10%

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\* This statement is opposite to that demonstrated clearly by Meuris et al. (26).

of that used in the conventional 5:1:1 SC-1 did not impair the desorption of Fe, Cu, Zn, and Ni from the Si surface. Meuris et al. (26) proposed a ratio of 5:1:0.25 as the best compromise for a modified SC-1 in terms of particle removal efficiency and avoidance of microroughening of the silicon. The authors who are cited in this paragraph have also examined the correlation between these effects, metal contamination, and electrical properties of grown oxide films (26)(27)(31)(138)-(140).

Sakurai et al. (141) reported that the thickness of the chemically grown oxide films on silicon during SC-1 cleaning does not depend on temperature, time, and solution composition (except for very low  $\text{NH}_4\text{OH}$  concentrations). The thickness of the films was 0.5 - 0.6 nm as determined by XPS analysis, or 1.2 nm, if measured by ellipsometry.

New results on wet-chemical contamination and on desorption cleaning by various processes and techniques were reported during this period by a number of researchers (19)-(31)(73)(139)(140)(143)-(153) as follows:

Heyns et al. (139) found that a dip of the wafers in dilute HF solution after SC-1/SC-2 removes any metal contaminants that may still be present, apparently without introducing new impurities (139). However, one has to be aware that post-cleaning exposure of the wafers to HF solutions will give rise to recontamination by organics, particles, and possibly trace metals. According to Rubloff (142), it should be applied only in the case of subsequent low-temperature epitaxial vapor growth where the absence of an oxide layer is crucial. Treatment by HF is not appropriate as a pre-oxidation clean where the formation of a passivating oxide layer is essential to prevent thermal surface etching and roughening of the silicon, with consequent degradation of the oxide qualities in MOS devices.

Verhaverbeke et al. (140) investigated the characteristics of HF-treated silicon surfaces as a function of immersion time in dilute HF solutions. They demonstrated the importance of forming a perfectly passivated surface, as evidenced by contact angle measurements, to reduce particle deposition. HF-last cleaning is more beneficial in terms of metallic contamination, as compared to RCA cleans. The improved processing has led to superior oxide integrity (140).

Grundner et al. (143) investigated surface composition and morphology of silicon wafers after HF solution treatments by means of instrumental surface analytical and angle-resolved light-scattering. Hirose et al. (144) studied the chemical stability and oxidation kinetics of H-terminated silicon surfaces after treatments in HF and BHF solutions, and Chabal (145) explored H-termination, atomic structure, and overall morphology.

Anttila and Tilli (146) showed that replacing SC-2 ( $\text{H}_2\text{O}-\text{H}_2\text{O}_2-\text{HCl}$ ) with very dilute ( $1:10^3$  to  $1:10^6$ ) acids, e.g.,  $1:10^4$   $\text{HCl}-\text{H}_2\text{O}$ , can remove several metallic contaminants (and metal hydroxides) without introducing as many particles as SC-2 does. The benefits of SC-1, which leaves the surface free of particles and organics, are combined with the benefits of immersion in dilute acids at room temperature, which remove metals efficiently without adding particles.

Kniffin et al. (147) showed that the type of chemical bonding of metallic impurities to the silicon surface plays an important role in determining the cleaning efficiency of a wet-chemical processing sequence. Poliak et al. (148) compared the effects of various wet-chemical cleaning sequences for removing metallic contaminants.

Shimono (149) demonstrated that an aqueous solution of 1%  $\text{H}_2\text{O}_2$  and 0.5% HF has a higher efficiency for removing metallic impurities than conventional cleans and also etches native oxide films on silicon. The improved effectiveness of this mixture is apparently based on the silicon surface etching action. Takizawa and Ohsawa (150) have used a similar approach by employing the classical  $\text{HNO}_3$ -HF silicon etchant in very dilute form (0.025 - 0.1% HF in  $\text{HNO}_3$ ), so that a silicon etch rate of 3 to 60 nm/min results without a substantial etching of thermal  $\text{SiO}_2$  patterns.

Hariri and Hockett (67) showed that replacing the  $\text{NH}_4\text{OH}$  in SC-1 with choline (trimethyl-2-hydroxyethyl ammonium hydroxide) plus a surfactant reduces oxidation-induced stacking faults in silicon better than RCA cleans do, and may also improve the removal of heavy metals, as noted in Sec. 3.3. Lowell (151) used the choline clean after a deglazing etch of doped polysilicon layers with dilute HF. The choline treatment generates a thin oxide film that prevents the formation of a contaminated oxide during rinsing. Menon et al. (152) showed, however, that if megasonic cleaning techniques are used, SC-1 is more effective for removing particles than choline solution. Syverson et al. (153) conducted temperature optimization tests for megasonic particle removal in SC-1/SC-2 which revealed that  $55^\circ\text{C}$  is the most effective temperature. Major reductions in wafer particle densities have been achieved by this optimized treatment in an advanced manufacturing environment. Many other aspects of particle contamination and its removal were covered extensively in the volumes of Refs. 10 and 11.

Tong et al. (44) reported that ozonized DI water used with conventional aqueous chemicals has good cleaning efficiency; concentrations of residual metals and particles were found to be equal or lower than after conventional RCA cleans. Matthews (45) carried the preparation of high-purity aqueous

chemicals from gaseous precursors a step further by using  $\text{NH}_3$  for preparing  $\text{NH}_4\text{OH}$  and  $\text{HCl}$  gas for  $\text{HCl}$  solutions, in addition to  $\text{O}_3$  for  $\text{H}_2\text{O}_2$ . This method of reagent synthesis will undoubtedly become an important future technology.

Finally, another important area related to wafer cleaning should be mentioned: reagent recycling and repurifying. Davison et al. (41) described the reprocessing, properties and application results of high-purity aqueous  $\text{HF}$ . Doshi et al. (154) state that impurity levels in this ion-exchange purified  $\text{HF}$  were routinely below 1 ppb for thirty-four elements and that it performed significantly better than the highest available purity of  $\text{HF}$ . (An MOS memory fab producing 1-Mbit DRAMs showed a 5% improvement in the wafer probe yield.) Davison (155)(156) and Hsu (42) have reviewed the technology of reprocessing or ultra-purifying both  $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$  (piranha etch) and aqueous  $\text{HF}$ .

**Vapor-Phase Cleaning Methods.** The basic approaches to dry or vapor-phase cleaning have been described in Sec. 3.6. Many of these approaches have been developed in this time period to the point of showing feasibility, as noted in Table 17. Only some selected outstanding highlight results will be briefly noted in this section. Many papers on this subject were included in the Proceedings volumes of Refs. 1 and 2.

**Table 17. Gas-Phase Cleaning Approaches**

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- |  |   |
|--|---|
| 1. Removal of Organic Contaminants by  | <ul style="list-style-type: none"> <li>▲ <math>\text{UV/O}_2</math> reaction</li> <li>▲ <math>\text{NO/HCl/N}_2</math> thermal reaction</li> <li>▲ Remote (downstream) plasma in <math>\text{O}_2</math></li> <li>▲ Plasma glow-discharge in <math>\text{H}_2</math></li> </ul>   |
| 2. Removal of Native Oxide Films       | <ul style="list-style-type: none"> <li>▲ <math>\text{HF}</math> vapor etching</li> <li>▲ Reduction annealing in <math>\text{H}_2</math></li> <li>▲ Low-energy ECR plasma etching in <math>\text{Ar}</math></li> <li>▲ Remote plasma exposure</li> </ul>   |
| 3. Removal of Metallic Contaminants by | <ul style="list-style-type: none"> <li>▲ <math>\text{UV/Cl}_2</math> microwave formation of <math>\text{Cl}</math> radicals</li> <li>▲ <math>\text{NO/HCl/N}_2</math> thermal reaction to form volatile nitrosyl compounds</li> <li>▲ Remote plasma discharge in <math>\text{HCl/Ar/O}_2</math></li> <li>▲ Formation of volatile metal halides</li> <li>▲ Formation of volatile metalorganics</li> <li>▲ Reaction with vapor-phase analogs of SC-1, SC-2</li> </ul> |
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The removal of native, grown, or deposited oxide films on silicon was accomplished before this review period by use of HF gas or vapor etching processes (126)-(128). The chemical mechanisms underlying these vapor-phase etching processes has been elucidated by Helms and Deal (157). Techniques and systems for implementing these processes and optimization of the vapor-phase etching reactions for oxide removal have been developed, investigated and reported during this period by many authors, e.g., Deal et al. (158), Ohmi et al. (159), Onishi et al. (160), Iscoff (161), Wong et al. (162), Nobinger et al. (163), and Deal and Helms (164). The addition of methanol instead of water vapor to anhydrous HF minimizes the formation of the solid reaction products encountered with the HF-H<sub>2</sub>O vapor etching systems, as observed by Izumi et al. (165).

Significant progress has been made by physical-chemical methods, such as glow discharge plasma reactions, for removing thin oxide films and certain contaminants on semiconductor wafers. Comfort (166) examined the thermodynamic parameters governing high-temperature thermal desorption and low-temperature oxide removal for pre-epitaxial surface cleaning of silicon. Reif (167) discussed in situ low-temperature cleaning for pre-epitaxial silicon growth; Liehr (168) examined the impact of silicon surface treatments prior to epitaxy and gate oxide growth, and Kalem et al. (169) reported on surface cleaning prior to the formation of SiO<sub>2</sub>/Si interfaces.

Tasch et al. (170) reviewed recent results on low-temperature in situ pre-epi cleaning of silicon by remote plasma-excited hydrogen in ultrahigh vacuum. Hattangady et al. (171) applied hydrogen, dissociated with remote noble-gas discharge, for the low-temperature cleaning of Ge and GaAs surfaces. Frystak and Ruzyllo (172) used remote plasma cleaning as a pre-oxidation treatment for silicon. Gas mixtures of O<sub>2</sub>, HCl/Ar, and NF<sub>3</sub>/H<sub>2</sub>/Ar were used to remove organics, metallic impurities, and thin oxide films, respectively. Finally, Chang (173) described an in situ plasma cleaning process for GaAs surfaces and device passivation.

Removal of metallic contaminants is best accomplished by thermal, chemical or photochemical vapor-phase reactions. Gluck (174) reported that nitric oxide can volatilize copper from silicon surfaces at 500°C, and gold reacts with a mixture of nitric oxide and HCl at 900 - 1000°C to form a volatilizable compound. The formation of volatile metal nitrosyl complex compounds with various metals and the NO-HCl-N<sub>2</sub> thermal reaction may be a promising approach to vapor-phase metal removal in general. Formation of volatile organometallic complexes with other reactants is quite possible. Ivankovits et al. (175) reported that reacting iron and copper on

silicon surface with 1,1,1,5,5,5-hexafluoro-2,4-pentanedione followed by volatilization at 300°C can reduce their concentrations. These early results look promising, but a great deal more work is needed to develop predictable and efficient processes.

Wong (176) reported results on a pre-oxidation treatment of silicon wafers with HCl/HF vapor mixtures, which were effective in reducing the detrimental effects caused by traces of heavy-metal contaminants; the oxide lifetime improved by 25%.

Low-temperature photochemical reactions have a great potential for transforming metallic contaminants into volatilizable compounds. Ultraviolet radiation is usually employed as the radiation source, for practical and energy considerations, with halogens as the reactants to generate highly reactive halogen radicals. Ito et al. (177)(178) utilized highly purified chlorine radicals to reduce the surface concentrations of Fe, Mg, Al, and Cu to levels lower than was possible with conventional wet cleans. Native oxide layers on silicon can be etched off with fluorine radicals generated by the same photo-activation process (178).

The well-known ultraviolet/ozone reaction for removing organic impurities from surfaces, reviewed by Vig (179), was applied to the cleaning of GaAs in epitaxial deposition processes by Pearton et al. (180) and by Kopf et al. (181) for the reduction of defects. Bedge and Lamb (182) studied the kinetics of the process and reported on experiments and modeling.

Finally, the status of particle removal by especially promising dry cleaning techniques is noted. McDermott et al. (183) described an argon-aerosol jet technique where frozen particles of argon are created and impinged at a high velocity on the wafer surface. Micron-size and submicron-size contaminant particles are dislodged by the collision energy and are entrained in the gas flow and removed from the system.

Bok et al. (184) reported on the theory and practice of a sophisticated method that is based on supercritical fluids, such as supercritical CO<sub>2</sub>. Their unique properties enables them to penetrate into deep IC structures and effect complete removal of particles and other contaminants. The supercritical liquid is first forced into trenches and crevices during compression in the pulsating pressure cycle. Subsequent expansion between supercritical and subcritical pressures dislodges particles and causes their ejection with a tremendous force.

Removal of particles in a vacuum system compatible with a dry cleaning sequence is technologically a great deal more difficult. Particle detachment by electrostatic techniques is ineffective. A promising technique

is based on the use of laser radiation. Allen (185)(186) has demonstrated that pulsed laser radiation is capable of effectively removing particles from surfaces. A moisture film is condensed between the particles and the wafer surface and is then explosively evaporated by a laser beam of an appropriately tuned wavelength. The dislodged particles can then be swept out of the system with a jet of inert gas.

## **5.0 SUMMARY AND CONCLUSIONS**

In the first part of this chapter we presented an overview of semiconductor wafer contamination aspects, discussing several important areas of technology that are directly or indirectly associated with wafer cleaning. We have shown that wafer cleaning technology in the broadest sense is interdisciplinary in that it involves not only surface chemical reactions in liquid and gas phases, but also chemical engineering to implement cleaning processes, contamination analysis by advanced instrumental methods for detecting and measuring trace impurities on surfaces and in chemicals, electrical measurements to determine the effects of contaminants on semiconductor devices, and the science of ultra-fine particles and their metrology. An understanding of the principles underlying these various disciplines is, therefore, important for successfully solving wafer cleaning problems in the laboratory and the fab.

In the second part we presented an overview of wafer cleaning technology in which we discussed in broad terms principles of liquid-phase cleaning processes and classifications of dry and vapor-phase cleaning methods.

The third part of the chapter was devoted to a chronological review in which we described the evolution of wafer cleaning science and technology from the early beginnings in the 1950s to the present time, mid-1992. The developments in the past three years have been truly "explosive", as judged by the number of scientific conferences and publications devoted to this topic.

We can conclude that the most widely used wafer cleaning methods in VLSI and ULSI silicon circuit fabrication are still, after twenty-five years, the hydrogen peroxide-based wet-chemical processes. High-purity reagents are now available, such as aluminum-free  $\text{H}_2\text{O}_2$ , that have led to improved performance results. However, the concentration of ammonium hydroxide in the original RCA SC-1 solution (5:1:1  $\text{H}_2\text{O}$ - $\text{H}_2\text{O}_2$ - $\text{NH}_4\text{OH}$ ) has



been reduced by at least four-fold to avoid micro-roughening of the silicon surface by nonuniform micro-etching, resulting in improved gate oxide integrity and increased yields of MOS capacitors. It is also advisable not to exceed 70°C for 10 min in the RCA SC-1/SC-2 wafer cleaning treatment. Removal of the native or chemical oxide film before and after SC-1 and SC-2 by optimized etching with dilute (1:50 - 1:100) ultrapure HF solution can be beneficial.

Remarkable results have also been achieved by wet-chemical cleaning of silicon wafers with aqueous solutions of choline-H<sub>2</sub>O<sub>2</sub>-surfactant, H<sub>2</sub>O-HF-HCl, H<sub>2</sub>O-H<sub>2</sub>O<sub>2</sub>-HF, very dilute acids, as well as with ozonized water. New techniques of wafer drying have been devised of which isopropyl alcohol vapor drying after cold DI water megasonic rinsing is one of the best.

While the use of advanced wet-chemical cleaning techniques for producing ultrapure silicon wafers will persist for at least several more years, the trend is toward a shift from liquid to gaseous reactants for several reasons. Removal of oxide layers by HF vapor-phase etching is now well established, and the elimination of organic contaminants by UV/ozone has been amply demonstrated. Processes for removing trace metals by vapor-phase analogs of SC-1 and SC-2 are being pursued vigorously. Possible solutions comprise photochemical complex formation with chlorine radicals generated from Cl<sub>2</sub> by UV radiation, thermal reaction and volatilization with NO/HCl/N<sub>2</sub> to produce volatile nitrosyl compounds, exposure to remote or downstream plasma discharges in HCl/Ar, and the formation of vacuum volatilizable metalorganic chelates or complexes. Electron cyclotron resonance plasma techniques have also been successful for removing contaminants. Particle elimination could be achieved by cryogenic techniques or by a new pulsed laser method that effectively dislodges particles so that they can be removed by a gas stream. Eventually and ideally, the entire cleaning sequence will be conducted in situ by a sequence of gas-phase reactions at low or reduced pressure and elevated temperature in a cluster tool that can be integrated with other cluster modules for film deposition, annealing, dry etching, and other processing steps.

## ACKNOWLEDGMENT

I wish to thank Dr. George L. Schnable for critically reviewing the draft of this chapter and for offering his many helpful comments.

## REFERENCES

1. *Proc. First International Symp. on Cleaning Technology in Semiconductor Device Manufacturing*, (J. Ruzyllo and R. E. Novak, eds.) Vol. 90-9, Electrochemical Society, Pennington, NJ (1990)
2. *Proc. Second International Symp. on Cleaning Technology in Semiconductor Device Manufacturing*, (J. Ruzyllo and R. E. Novak, eds.) Vol 92-12, Electrochemical Society, Pennington, NJ (1992)
3. *Semicon/Korea '91 Tech. Proc.*, Seoul, Korea. SEMI, Mountain View, CA (Sept. 26-27, 1991)
4. *Semicon/Europe '92 Tech. Proc.*, Zurich, Switzerland. SEMI, Mountain View, CA (March 10-11, 1992)
5. *Proc. on Chemical Surface Preparation, Passivation, and Cleaning, Growth and Processing, Symp. B*, Spring Mtg. of the Materials Research Society (MRS), San Francisco, CA (April 12-16, 1992)
6. *Proc. of the Ann. Tech. Mtgs. of the Institute of Environmental Sciences*, Mount Prospect, IL; and *Ann. Microcontamination Conf. Proc.*, sponsored by Microcontamination Magazine (1990, 1991, 1992)
7. *Proc. of the Semiconductor Pure Water and Chemicals Conf.*, Santa Clara, CA. Balazs Analytical Laboratory, Sunnyvale, CA (Feb 11-13, 1992)
8. *Electrochemical Society (ECS) Ext. Abstr.* (a) Vol. 90-1 (1990); (b) Vol. 90-2 (1990); (c) Vol. 91-1 (1991); (d) Vol. 91-2 (1991); (e) Vol. 92-1 (1992). Electrochemical Society, Pennington, NJ
9. *Handbook of Contamination Control in Microelectronics*, (D. L. Tolliver, ed.), Noyes Publications, Park Ridge, NJ (1988)
10. *Particles on Surfaces*, Vols. 1 and 2, (K. L. Mittal, ed.), Plenum Publishing Corp., New York (1988 and 1989); *Particles in Gases and Liquids*, Vols. 1 and 2, (K. L. Mittal, ed.), Plenum Publishing Corp., New York (1989 and 1990)
11. *Particle Control for Semiconductor Manufacturing*. (R. P. Donovan, ed.), M. Dekker Inc., New York (1990)
12. Slusser, G. J. and MacDowell, L., *J. Vac. Sci. Technol.* A-5 (4):1649-1651 (1987)
13. Monkowski, J. R., *Treatise on Clean Surfaces Technology*, (K. L. Mittal, ed.), Vol. 1, Ch. 6, pp. 123-148, Plenum Press, New York (1987)
14. Khilnani, A., *Particles on Surfaces 1: Detection, Adhesion, and Removal*, (K. L. Mittal, ed.) pp. 17-35, Plenum Press, New York (1988)

15. Burkman, D. C., Peterson, C. A., Zazzera, L. A., and Kopp, R. J., *Microcontamination* 6(11):57-62, 107-111 (1988)
16. Atsumi, J., Ohtsuka, S., Munehira, S., and Kajiyama, K., pp. 59-66 in Ref. 1
17. Hattori, T., *Solid State Technol.* 33(7):S1-S8 (1990)
18. Jastrzebski, L., *ECS Ext. Abstr.*, 90-1:587-588, Electrochemical Society, Pennington, NJ (1990)
19. Riley, D., and Carbonell, R., *Proc. of The Institute of Environmental Sciences Ann. Tech. Mtg.*, pp. 224-228, New Orleans, LA (1990)
20. Ohsawa, A., Honda, K., Takizawa, R., Nakanishi, T., Aoki, M. and Toyokura, N., *Proc. Sixth International Symp. on Silicon Materials Science and Technology*, (Huff, Barraclough, and Chikawa, eds.) 90-7:601-613, Electrochemical Society, Pennington, NJ (1990)
21. Matsushita, Y., and Tsuchya, N., *ECS Ext. Abstr.*, 90-2:601, Electrochemical Society, Pennington, NJ (1990)
22. Kern, F., Jr., Mitsushi, I., Kawanabe, I., Miyashita, M., Rosenberg, R. W., Ohmi, T., *Proc. of the 37th Ann. Tech. Mtg.*, Institute of Environmental Sciences, San Diego, CA (1991)
23. Riley, D. J., and Carbonell, R. G., *Proc. of the 37th Ann. Tech. Mtg.*, pp. 886-891, Institute of Environmental Sciences, San Diego, CA (1991)
24. Meuris, M., Heyns, M., Küper, W., Verhaverbeke, S., and Philipossian, A., *ECS Ext. Abstr.*, 91-1:488, Electrochemical Society, Pennington, NJ (1991)
25. Bergholz, W., Zoth, G., Gelsdorf, F., and Kolbesen, B., *ECS Ext. Abstr.* 91-1:227-228, Electrochemical Society, Pennington, NJ. (1991)
26. Meuris, M., Heyns, M., Mertens, P., Verhaverbeke, S., and Philipossian, A., pp. 144-161 in Ref. 2
27. Verhaverbeke, S., Meuris, M., Mertens, P. W., Kelleher, A., Heyns, M. M., De Keersmaecker, R. F., Murrell, M., and Sofield, C. J., pp. 187-196 in Ref. 2
28. Tonti, A., pp. 409-417 in Ref. 2
29. Gupta, P., Van Horn, M., and Frost, M., in *Proc. of the Semiconductor Pure Water and Chemicals Conf.*, Santa Clara, CA., pp. 191-198, Balazs Analytical Laboratory, Sunnyvale, CA (Feb 11-13, 1992)
30. Anttila, O. J., Tilli, M. V., Schaekers, M., and Claeys, C. L., *J. Electrochem. Soc.* 139:1180-1185 (1992)

31. Verhaverbeke, S., Mertens, P. W., Meuris, M., Heyns, M. M., Schnegg, A., and Philipossian, A., in *Semicon/Europe '92 Tech. Proc.*, Zurich, Switzerland. SEMI, Mountain View, CA (March 10-11, 1992)
32. Kern, W., in *Semicon/Korea '91 Tech. Proc.*, Seoul, Korea, Session III, pp. 39-88, SEMI, Mountain View, CA (Sept. 26-27, 1991)
33. Osburn, C. M., *Microcontamination* 9(7):19-27, 76 (1991)
34. Dillenbeck, K., *Particle Control for Semiconductor Manufacturing*. (R. P. Donovan, ed.), Ch. 15, pp. 255-261, M. Dekker Inc., New York (1990)
35. Ohmi, T., Inaba, H., and Takenami, T., *Microcontamination* 7(10):29-32, 86-97 (1989)
36. Fisher, W. G., *Particle Control for Semiconductor Manufacturing*. (R. P. Donovan, ed.), pp. 415-428, M. Dekker Inc., New York (1990)
37. Kern, W., Keynote lecture presented at the Semiconductor Pure Water and Chemicals Conf., Santa Clara, CA. Balazs Analytical Laboratory, Sunnyvale, CA, (Feb 11-13, 1992)
38. Hashimoto, S., Kaya, M., and Ohmi, T., *Microcontamination*, 7(6): 25-28, 98-106 (1989)
39. Harder, N., *Solid State Technol.*, 33(10):S1-S4 (1990)
40. Naggan, M., *Handbook of Contamination Control in Microelectronics*, (D. L. Tolliver, ed.), Ch. 11, Noyes Publications, Park Ridge, NJ (1988)
41. Davison, J., Hsu, C., Trautman, E., and Lee, H., pp. 83-91 in Ref. 1
42. Hsu, C., *Chemical Proc. of the Semiconductor Pure Water and Chemicals Conf.*, pp. 44-62, Santa Clara, CA. Balazs Analytical Laboratory, Sunnyvale, CA (Feb 11-13, 1992)
43. Krusell, W. C., and Golland, D. I., pp. 23-32 in Ref. 1: see also original O<sub>3</sub>-work by W. C. Krusell et al., *ECS Ext. Abstr.*, 86-1:133 (1986)
44. Tong, J. K., Grant, D. C., and Peterson, C. A., pp. 18-25 in Ref. 2
45. Matthews, R. R., *Chemical Proc. of the Semiconductor Pure Water and Chemicals Conf.*, pp. 3-15, Santa Clara, CA. Balazs Analytical Laboratory, Sunnyvale, CA (Feb 11-13, 1992)
46. Faylor, T. L., and Gorski, J. J., *Handbook of Contamination Control in Microelectronics*, (D. L. Tolliver, ed.), Ch. 6, Noyes Publications, Park Ridge, NJ (1988)
47. Sinha, D., *Solid State Technol.*, 35(3):S9-S12 (1992)
48. Monkowski, J. R., Freeman, D. W., *Solid State Technol.*, 33(7):S13-S17 (1990)

49. Hockett, R. S., pp. 227-242 in Ref. 1. See also: *Semicon/Korea '91 Tech. Proc.*, Seoul, Korea. Ch. III, pp. 89-98, SEMI, Mountain View, CA (Sept. 26-27, 1991)
50. Kamieniecki, E., pp 273-279 in Ref. 1
51. Zoth, G., and Bergholz, W., *ECS Ext. Abstr.*, 91-2:643-644, Electrochemical Society, Pennington, NJ. (1991)
52. Hahn, S., Eichinger, P., Park, J-G., Kwack, Y-S., Cho, K-C., and Choi, S-P., *Semicon/Korea '91 Tech. Proc.*, Seoul, Korea. Session III, pp. 60-78, SEMI, Mountain View, CA (Sept. 26-27, 1991)
53. Shimura, F., *Semicon/Korea '91 Tech. Proc.*, Seoul, Korea. Session III, pp. 23-34, SEMI, Mountain View, CA (Sept. 26-27, 1991)
54. Gupta, P., and Frost, M., *Proc. on Chemical Surface Preparation, Passivation, and Cleaning, Growth and Processing, Symp. B*, Paper B5.10, Spring Mtg. of MRS, San Francisco, CA (April 12-16, 1992)
55. Jastrzebski, L., Milic, O., Dexter, M., Lagowski, J., DeBusk, D., Nauka, K., Mitowski, R., Gordan, R., and Persson, E., pp 294-313 in Ref. 2
56. Rathmann, D., pp 338-343 in Ref. 2
57. Grundner, M., Hahn, P. O., Lampert, I., Schnegg, A., and Jacob, H., pp. 215-226 in Ref. 1
58. Kern, W., and Deckert, C. A., *Thin Film Processes*, (J. L. Vossen and W. Kern, eds.) Ch. V-1, pp. 401-496, Academic Press, New York (1978)
59. Kern, W., and Schnable, G. L., *The Chemistry of the Semiconductor Industry*, (S. J. Moss and A. Ledwith, eds.) Ch. 11, pp. 223-276, Chapman and Hall, New York (1987)
60. Walker, P., and Tarn, W. H., *CRC Handbook of Etchants for Metals and Metallic Compounds*, CRC Press, Inc., Boca Raton, FL (1990)
61. *Quick Reference Manual for Silicon Integrated Circuit Technology*, (W. E. Beadle, J. C. C. Tsai and R. D. Plummer, eds.) John Wiley and Sons, New York (1985)
62. Kern, W., *Semicond. International* 7(4):94-99 (1984)
63. Kern, W., *J. Electrochem Soc.* 137:1887-1892 (1990); also pp. 3-19 in Ref. 1
64. Kern, W., Puotinen, D., *RCA Review* 31:187-206 (1970)
65. Muraoka, H., Kurosawa, K. J., Hiratsuka, H., and Usami, T., *ECS Ext. Abstr.*, 81-2:570-573 (1981)
66. Park, J. G., and Raghavan, S., pp. 26-33 in Ref. 2

67. Hariri, A., and Hockett, R. S., *Semicond. International* 12(9):74-78 (1989)
68. Skidmore, K., *Semicond. International*, 10(9):80-85 (1987)
69. Skidmore, K., *Semicond. International*, 12(8):80-86 (1989)
70. Burggraaf, P., *Semicond. International*, 13(11):52-58 (1990)
71. Busnaina, A. A., and Kern, F. W., Jr., *Solid State Technol*, 30(11):111-114 (1987)
72. Menon, V. B., Clayton, A. C., and Donovan, R. P., *Microcontamination* 7(6):31-34, 107-108 (1989)
73. Tonti, A., pp. 41-47 in Ref. 2
74. Burkman, D., *Semicond. International*, 4(7):103-116 (1981)
75. McConnell, C. F., *Microcontamination*, 9(2):35-40 (1991)
76. Mayer, A., Shwartzman, S., *J. Electronic Materials*, 8:885-864 (1979)
77. Shwartzman, S., Mayer, A., and Kern, W., *RCA Review*, 46:81-105 (1985)
78. Ohmi, T., Mishima, H., Mizuniwa, T., and Abe, M., *Microcontamination*, 7(5):25-32, 108 (1989)
79. Mishima, H., Ohmi, T., Mizuniwa, T., and Abe, M., *IEEE Trans. on Semiconductor Manufacturing*, 2(4):121 (1989)
80. Mishima, H., Yasui, T., Mizuniwa, T., Abe, M., and Ohmi, T., *IEEE Trans. on Semiconductor Manufacturing*, 2(3):69 (1989)
81. McConnell, C. F., *Microcontamination*, 9(2):35-40 (1991)
82. Olesen, M. B., *Proc. Institute of Environmental Sciences, Ann. Tech. Mtg.*, pp. 229-241, Mount Prospect, IL (1990)
83. Anabuki, K., Yamashita, Y., and Nawata, T., *ECS Ext. Abstr.*, 90-2:443, Electrochemical Society, Pennington, NJ. (1990)
84. Marra, J., *Ext. Abstr., Third Symp. on Particles in Gases and Liquids: Detection, Characterization and Control*, p. 52, San Jose, CA (1991)
85. Oki, I., Biwa, T., Kudo, J., and Ashida, T., pp. 215-222 in Ref. 2
86. Koontz, D. E., Thomas, C. O., Craft, W. H., and Amron, I., *Symp. on Cleaning of Electronic Device Components and Materials*, ASTM STP No. 246, pp. 136-145 (1959)
87. Feder, D. O., and Koontz, D. E., *Symp. on Cleaning of Electronic Device Components and Materials*, ASTM STP No 246, pp. 40-65 (1959)

## 62 Handbook of Semiconductor Wafer Cleaning Technology

88. Wolsky, S. P., Rodriguez, P. M., and Waring, W., *J. Electrochem Soc.* 103:606 (1956)
89. Sotnikov, V. S., and Belanovskii, A. S., *Russian J. of Phys. Chem.* 34:1001-1003 (1960)
90. Larrabee, G. B., *J. Electrochem Soc.* 108:1130-1134 (1961)
91. Kern, W., *Semiconductor Products* (early name for *Solid State Technology*), Vol. 6, Part I, 22-26 (Oct. 1963); Part II, 23-27 (Nov. 1963)
92. Kern, W., *RCA Engineer* 9(3): 62-66 (1963)
93. Kern, W., *RCA Review*, Part I: 31:207-233, (1970); Part II: 31:234-264 (1970); Part III: 32:64-87 (1971)
94. Kern, W., *Solid State Technol.* 15, Part I: (1)34-38 (1972); Part II: (2)39-45 (1972)
95. Kern, W., *J. Electrochem Soc.* 109:700-705 (1962)
96. Henderson, R. C., *J. Electrochem. Soc.* 119:772-775 (1972)
97. Meek, R. L., Buck, T. M., and Gibbon, C. F., *J. Electrochem. Soc.*, 120:1241-1246 (1973)
98. Amick, J. A., *Solid State Technol.* 47(11):47-52 (1976)
99. Murarka, S. P., Levinstein, H. J., Marcus, R. B., and Wagner, R. S., *J. Appl. Phys.* 48:4001-4003 (1979)
100. Gluck, R. M., *ECS Ext. Abstr.* 78-2:640 (1978)
101. Peters, D. A., and Deckert, C. A., *J. Electrochem. Soc.*, 126:883-886 (1979)
102. Phillips, B. F., Burkman, D. C., Schmidt, W. R., and Peterson, C. A., *J. Vac. Sci. Technol.*, A-1(2):646-649 (1983)
103. Goodman, A. M., Goodman, L. A., and Gossenberger, H. F., *RCA Review*, 44(2):326-341 (1983)
104. Kern, W., *RCA Engineer*, 28(4):99-105 (1983)
105. Watanabe, M., Harazono, M., Hiratsuka, Y., and Edamura, T., *ECS Ext. Abstr.*, 83-1:221-222 (1983)
106. Bansal, I. K., *Microcontamination*, 2(4):35-40 (1984)
107. Bansal, I. K., *Solid State Technol.*, 29(7):75-80 (1986)
108. Ishizaka, A., and Shiraki, Y., *J. Electrochem. Soc.*, 133(4):666-671 (1986)
109. Wong, C. Y., and Klepner, S. P., *Appl. Phys. Lett.*, 48(18):1229-1230 (1986)
110. Grundner, M., and Jacob, H., *Appl. Phys.*, A-39:73-82 (1986)

111. Becker, D. S., Schmidt, W. R., Peterson, C. A., and Burkman, D., *Microelectronics Processing: Inorganic Materials Characterization*, (L. A. Casper, ed.), Ch. 23, pp. 368-376, ACS Symp. Series No. 295, American Chemical Society (1986)
112. Kawado, S., Tanigaki, T., and Maruyama, T., *Semiconductor Silicon 1986, Proc. Fifth International Symp. on Silicon Mater. Sci. Technol.*, (H. R. Huff, T. Abe, and B. Kolbesen, eds.), pp. 989-998, Electrochemical Society, Pennington, NJ (1986)
113. McGillivray, I. G., Robertson, J. M., and Walton, A. J., *Semiconductor Silicon 1986, Proc. Fifth International Symp. on Silicon Mater. Sci. Technol.*, (H. R. Huff, T. Abe, and B. Kolbesen, eds.), pp. 999-1010, Electrochemical Society, Pennington, NJ (1986)
114. Lampert, I., *ECS Ext. Abstr.*, 87-1:381-382 (1987)
115. Gould, G., and Irene, E. A., *J. Electrochem. Soc.*, 174(4):1031-1033 (1987)
116. Ruzyllo, J., *J. Electrochem. Soc.*, 174(4):1869-1870 (1987)
117. Probst, V., Bohm, H. J., Schaber, H., Oppolzer, H., and Weitzel, I., *J. Electrochem. Soc.*, 135(3):671-676 (1988)
118. Peterson, C. A., *Particles on Surfaces 1: Detection, Adhesion, and Removal*, (K. L. Mittal, ed.), pp. 37-42, Plenum Press, New York (1988)
119. Morita, E., Yoshimi, T., and Shimanuki, Y., *ECS Ext. Abstr.*, 89-1:352-353 (1989)
120. Yoshimi, T., Morita, E., and Shimanuki, Y., *ECS Ext. Abstr.*, 89-1:354-355 (1989)
121. Gould, G., and Irene, E. A., *J. Electrochem. Soc.*, 136(4):1108-1112 (1989)
122. Bowling, R. A., *J. Electrochem. Soc.*, 132(9):2208-2214 (1985)
123. Menon, V. B., Michaels, L. D., Donovan, R. P., Hollar, L. A., and Ensor, D. S., *Proc. Institute of Environmental Sciences, Ann. Mtg.*, King of Prussia, PA. (May 2-6, 1988)
124. Vig, J. R., *Treatise on Clean Surface Technology*, (K. L. Mittal, ed.), Vol. 1, pp. 1-26, Plenum Press, New York (1987)
125. Kaneko, T., Suemitsu, M., and Miyamoto, N., *Jpn. J. of Appl. Phys.* 28(12):2425-2429 (1989).
126. Claevelin, C. R., and Duranko, G. T., *Semicond. International*, 10(12):94-99 (1987); Novak, R. E. *Solid State Technol.*, 31(3):39-41 (1988)
127. Clements, L. D., Busse, J. E., and Mehta, J., *Semicond. Fabrication Technology and Metrology, ASTM STP 990*, (D. C. Gupta, ed.), ASTM, Philadelphia, PA (1988)



128. Duranko, G., Syverson, D., Zazzera, L., Ruzyllo, J., and Frystak, D., *Physics and Chemistry of SiO<sub>2</sub> and Si-SiO<sub>2</sub> Interface* (B. E. Deal and C. R. Helms, eds.), pp. 429-436, Plenum Publishing Corp., New York (1988)
129. Fountain, G. G., Hattangady, S. V., Rudder, R. A., Posthill, J. B., and Markunas, R. J., *MRS Symp. Proc.* 146:139 (1989)
130. Burrows, V. A., Chabal, Y. J., Higashi, G. S., Raghavachari, K. and Christman, S. B., *Appl. Phys. Lett.*, 53(11):998-1000 (1988)
131. Hahn, P. O., Grundner, M., Schnegg, A., and Jacob, H., *Appl. Surf. Sci.*, 39:436 (1989)
132. Zazzera, L. A., and Moulder, J. F., *J. Electrochem Soc.*, 136(2):484-491 (1989)
133. Chabal, Y. J., Higashi, G. S., Raghavachari, K., and Burrows, V. A., *J. Vac. Sci. Technol. A*7(3):2104-2109 (1989)
134. van den Meerakker, J. E. A. M. and van der Straaten, M. H. M., *J. Electrochem. Soc.* 37:1239-1243 (1990)
135. Tanaka, K., Sakurai, M., Kamizuma, S., and Shimanuki, Y., *ECS Ext. Abstr.* 90-1:689-690, Electrochemical Society, Pennington, NJ. (1990)
136. Miyashita, M., Itano, M., Imaoka, T., Kawanabe, I., and Ohmi, T., *ECS Ext. Abstr.* 91-1:709-710, Electrochemical Society, Pennington, NJ (1991)
137. Ohmi, T., Tsuga, T., and Takano, J., *ECS Ext. Abstr.* 92-1:388-389, Electrochemical Society, Pennington, NJ (1992)
138. Ohmi, T., *ECS Ext. Abstr.* 91-1:276-277, Electrochemical Society, Pennington, NJ. (1991)
139. Heyns, M., Hasenack, C., De Keersmaecker, R., and Falster, R., *Microelectronic Engineering* 10:235-257 (1991); also: Heyns, M. M., *Microcontamination*, 9(4): 29-34, 87-89 (1991)
140. Verhaverbeke, S., Alay, J., Mertens, P., Meuris, M., Heyns, M., Vandervorst, W., Murrell M., and Sofield, C., *Proc. on Chemical Surface Preparation, Passivation, and Cleaning, Growth and Processing, Symp. B*, Spring Mtg. of MRS, San Francisco, CA (April 12-16, 1992)
141. Sakurai, M., Ryuta, J., Morita, E., Tanaka, K., Yoshimi, T., and Shimanuki, Y., *ECS Ext. Abstr.*, 90-1:710-711, Electrochemical Society, Pennington, NJ (1990)
142. Rubloff, G. W., *SEMICON/Korea '90 Tech. Proc.*, pp. 2-3 to 11, SEMI, Mountain View, CA (Dec, 6-7, 1990)

143. Grundner, M., Gräf, D., Hahn, P. O., and Schnegg, A., *Solid State Technol.*, 34(2):69-75 (1991)
144. Hirose, M., Yasaka, T., Kanda, K., Takakura, M., and Miyazaki, S., pp. 1-9 in Ref. 2
145. Chabal, Y. J., *Proc. on Chemical Surface Preparation, Passivation, and Cleaning, Growth and Processing, Symp. B*, Paper 6.1, Spring Mtg. of MRS, San Francisco, CA (April 12-16, 1992)
146. Anttila, O. J., and Tilli, M. V., pp. 179-189 in Ref. 2; *J. Electrochem. Soc.* 139:1751-1756 (1992)
147. Kniffin, M. L., Beerling, T. E., and Helms, C. R., *J. Electrochem. Soc.*, 139:1195-1199 (1992)
148. Poliak, R., Matthews, R., Gupta, P. K., Frost, M., and Triplett, B., *Microelectronics*, 10(6):45-49, 93-94 (1992)
149. Shimono, T., *ECS Ext. Abstr.*, 91-1:278-279, Electrochemical Society, Pennington, NJ. (1991)
150. Takizawa, R., and Ohsawa, A., pp. 75-82 in Ref. 1
151. Lowell, L., *Solid State Technol.*, 34(4):149-152 (1991)
152. Menon, V. B., and Donovan, R. P., pp. 167-181 in Ref. 1. Also: *Microcontamination*, 8(11):29-34, 66 (1990)
153. Syverson, W. A., Fleming, M. J., and Schubring, P. J., pp. 10-17 in Ref. 1
154. Doshi, V., Hall, L., and Davison, J., *Defect Reduction in DRAM Manufacture using Ion Exchange-Purified HF*, Paper to be presented at the Fall Mtg. of the Electrochemical Society, Toronto, Ontario, Canada (Oct. 12-16, 1992); *ECS Ext. Abstr.*, 92-2, Abstract No. 410 (1992)
155. Davison, J., *Solid State Technol.*, 35(3):S1-S5 (1992)
156. Davison, J., *Solid State Technol.*, 35(7):S10-S14 (1992)
157. Helms, C. R., and Deal, B. E., pp. 267-276 in Ref. 2
158. Deal, B. E., McNeilly, M., Kao, D. B., and deLarios, J. M., pp. 121-128 in Ref. 1; also: *Solid State Technol.*, 33(7):73-77 (1990)
159. Ohmi, T., Miki, N., Kikuyama, H., Kawanabe, I., and Miyashita, M., pp. 95-104 in Ref. 1
160. Onishi, S., Matsuda, K., and Sakiyama, K., *ECS Ext. Abstr.*, 91-1:519-520, Electrochemical Society, Pennington, NJ. (1991)
161. Iscoff, R., *Semicond. International*, 14(12):50-54 (1991)

162. Wong, M., Moslehi, M. M., and Reed, D. W., *J. Electrochem. Soc.*, 138:1799-1802 (1991)
163. Nobinger, G. L., Moskowitz, D. J., and Krusell, W. C., *Microcontamination*, 10(4):21-26, 68-69 (1992)
164. Deal, B. E., and Helms, C. R., *Proc. on Chemical Surface Preparation, Passivation, and Cleaning, Growth and Processing, Symp. B*, Paper 6.2, Spring Mtg. of MRS, San Francisco, CA (April 12-16, 1992)
165. Izumi, A., Matsuka, T., Takeuchi, T., and Yamano, A., pp. 260-266 in Ref. 2
166. Comfort, J. H., pp. 428-436 in Ref. 2
167. Reif, R., *Proc. on Chemical Surface Preparation, Passivation, and Cleaning, Growth and Processing, Symp. B*, Paper 7.1, Spring Mtg. of MRS, San Francisco, CA (April 12-16, 1992)
168. Liehr, M., *Proc. on Chemical Surface Preparation, Passivation, and Cleaning, Growth and Processing, Symp. B*, Paper 1.1, Spring Mtg. of MRS, San Francisco, CA (April 12-16, 1992)
169. Kalem, S., Lamb, H. H., Yasuda, T., Ma, Y., and Lucovsky, G., *Proc. on Chemical Surface Preparation, Passivation, and Cleaning, Growth and Processing, Symp. B*, Paper 2.2, Spring Mtg. of MRS, San Francisco, CA (April 12-16, 1992)
170. Tasch, A., Banerjee, S., Hsu, T., Qian, R., Kinosky, D., Irby, J., Mahajan, A., and Thomas, S., *Proc. on Chemical Surface Preparation, Passivation, and Cleaning, Growth and Processing, Symp. B*, Paper 1.4, Spring Mtg. of MRS, San Francisco, CA (April 12-16, 1992); see also: pp. 418-427 in Ref. 2
171. Hattangady, S. V., Rudder, R. A., Mantini, M. J., Fountain, G. G., Posthill, J. B., and Markunas, R. J., *MRS Symp. Proc.*, 165:221-226 (1990)
172. Frystak, D., and Ruzyllo, J., pp. 58-71 in Ref. 2
173. Chang, E. Y., *Proc. on Chemical Surface Preparation, Passivation, and Cleaning, Growth and Processing, Symp. B*, Paper 5-18, Spring Mtg. of MRS, San Francisco, CA (April 12-16, 1992)
174. Gluck, R. M., pp. 48-57 in Ref. 2
175. Ivankovits, J. C., Bohling, D. A., Lane, A., and Roberts, D. A., pp. 105-111 in Ref. 2
176. Wong, J., Liu, D., Moslehi, M., and Reed, D., *Electron Dev. Lett.*, 12:425 (1991)

177. Ito, T., Sugino, R., Watanabe, S., Nara, Y., and Sato, Y., pp. 114-120 in Ref. 1
178. Ito, T., Sugino, R., Sato, Y., Okuno, M., Osawa, A., Aoyama, T., Yamazaki, T., and Arimoto, Y., *Proc. on Chemical Surface Preparation, Passivation, and Cleaning, Growth and Processing, Symp. B*, Paper 3.1, Spring Mtg. of MRS, San Francisco, CA (April 12-16, 1992). Also: *Semicon/Korea '91 Tech. Proc.*, Seoul, Korea. Session III, pp. 44-52, SEMI, Mountain View, CA (Sept. 26-27, 1991)
179. Vig, J. R., pp. 105-113 in Ref. 1
180. Pearton, S. J., Ren, F., Abernathy, C. R., Hobson, W. S., and Luftman, H. S., *Appl. Phys. Lett.*, 58(13):1416-1418 (April 1, 1990)
181. Kopf, R. F., Kinsella, A. P., and Ebert, C. W., *J. Vac. Sci. Technol.*, B9(1):132-135 (1991)
182. Bedge, S., and Lamb, H. H., *Proc. on Chemical Surface Preparation, Passivation, and Cleaning, Growth and Processing, Symp. B*, Paper 3.2, Spring Mtg of MRS, San Francisco, CA (April 12-16, 1992)
183. McDermott, W. T., Ockovic, R. C., Wu, J. J., and Miller, R. J., *Microcontamination*, 9(10):33-36, 94-95 (1991)
184. Bok, E., Kelch, D., and Schumacher, K. S., *Solid State Technol.*, 35(6):117-120 (1992)
185. Allen, S. D., *Scientific American*, 26(6):86-87 (1990)
186. Allen, S. D., "Laser Assisted Particle Removal," Tech. Report, University of Iowa (1990); see also: Lee, S. J., Imen, K., and Allen, S. D., Paper EM-WeM10, presented at the American Vacuum Society National Symp., Seattle, WA (Nov. 11-15, 1991)

## **Part II.**

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# **Wet-Chemical Processes**

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## Aqueous Cleaning Processes

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***Don C. Burkman, Donald Deal, Donald C. Grant,  
and Charlie A. Peterson***

### **1.0 INTRODUCTION TO AQUEOUS CLEANING**

The purpose of this chapter is to draw attention to the important considerations in aqueous cleaning of semiconductor surfaces.

The basic requirement for cleaning processes is the removal of contamination. Such removal is of paramount importance to semiconductor chip manufacturers since it is generally accepted that over 50% of yield losses in integrated circuit fabrication are due to microcontamination. Furthermore, any metals left on the surface may spread and diffuse into the semiconductor interior and cause yield loss and/or loss of chip function reliability. Whether the contaminants are specific or general, or whether the source of the contaminants is known or unknown, the successful removal of contamination is the essence of cleaning.

Aqueous chemistries involve a variety of solutions which can be made by dissolving a gas, liquid, or solid in water. Aqueous cleaning solutions are currently the most widely used due to their many advantages over alternative processes. Alternatives include cleaning with organic solvents, and the application of vapor phase chemistries (both organic and inorganic), as well as the use of various physical and thermal methods of contaminant removal. Some of the advantages and disadvantages of aqueous cleaning are listed below.

### **1.1 Advantages of Aqueous Cleaning:**

- Rinsing is easily accomplished in water
- Residues left after drying can be avoided by deionized water rinsing and suitable drying
- Flammability hazard is low or non-existent
- Disposal of a large variety of aqueous chemicals has low environmental impact
- A wide range of chemicals is available
- Many aqueous chemicals are low cost
- Aqueous chemistries are capable of removing organics and inorganics to very low levels
- Aqueous solutions generally have lower vapor pressure than organic solvents
- In most cases aqueous chemicals have very high reaction selectivity between the contaminants to be removed and surfaces being cleaned

### **1.2 Disadvantages of Aqueous Cleaning:**

- Drying is not as fast or as easy as with organic solvents due to the low vapor pressure of water. Incorrect drying can result in recontamination
- Some organic solvents are more efficient for removing certain organic contaminants
- Aqueous chemicals can be dangerous to handle, breathe, etc.
- Disposal of some aqueous chemicals is difficult and can be expensive
- Aqueous systems are difficult to couple to vacuum systems

Since there are many applications requiring aqueous cleaning in semiconductor manufacturing, with widely differing demands for surface cleanliness, not all of these considerations are important to each application. Nevertheless, in an attempt to address the most pertinent issues, the information in this chapter has been organized under the following headings:

1. Introduction to Aqueous Cleaning
2. Considerations of Contaminants and Substrates

3. Factors Affecting Aqueous Cleaning
4. Cleaning Chemistries
5. An Example of an Aqueous Chemical Cleaning Process
6. The Effect of Process Variables on Aqueous Chemical Cleaning
7. Semiconductor Wafer Drying
8. Equipment Used For Aqueous Cleaning
9. Conclusion

## **2.0 CONSIDERATIONS OF CONTAMINANTS AND SUBSTRATES**

In order to obtain the desired clean surface, it is necessary to remove all contamination and to prevent it from re-establishing residence on the wafer surface prior to use or the next operation. Contaminants may occur as films or as particles on the surface. They may also be incorporated in the top layers of the wafer surface. The contaminants may be either organic or inorganic in composition. The cleaning procedure must be designed to address both the chemical type (organic or inorganic) and the physical form (film, particulate, or surface incorporated) of the contamination.

Organic contaminants may originate from a variety of sources, such as lubricants, coolants, cutting oils, fatty materials from human handling, airborne particles, detergents, corrosion inhibitors, and organic residues. These organic residues are most commonly found after evaporation of organic solvents on the wafer surface. This surface deposition can also occur during evaporation of aqueous solutions and during the dilution associated with water rinsing. Aqueous solutions are likely to leave behind inorganic species as well.

Evaporative deposition of organics can occur during solvent evaporation. A carboxyl group, if present in the residue, is generally physically adsorbed to the surface whereas the hydrocarbon portion orients itself away from the surface. Following the physical adsorption of the molecule, it is possible to have a chemical reaction between the functional group (carboxyl group in this example) and the wafer surface. When this happens, the molecule is said to be chemisorbed (1).

Physical methods of scrubbing, spraying, or ultrasonics alone are generally ineffective in removing chemisorbed materials. These materials must be removed chemically or by removal of some of the surface.

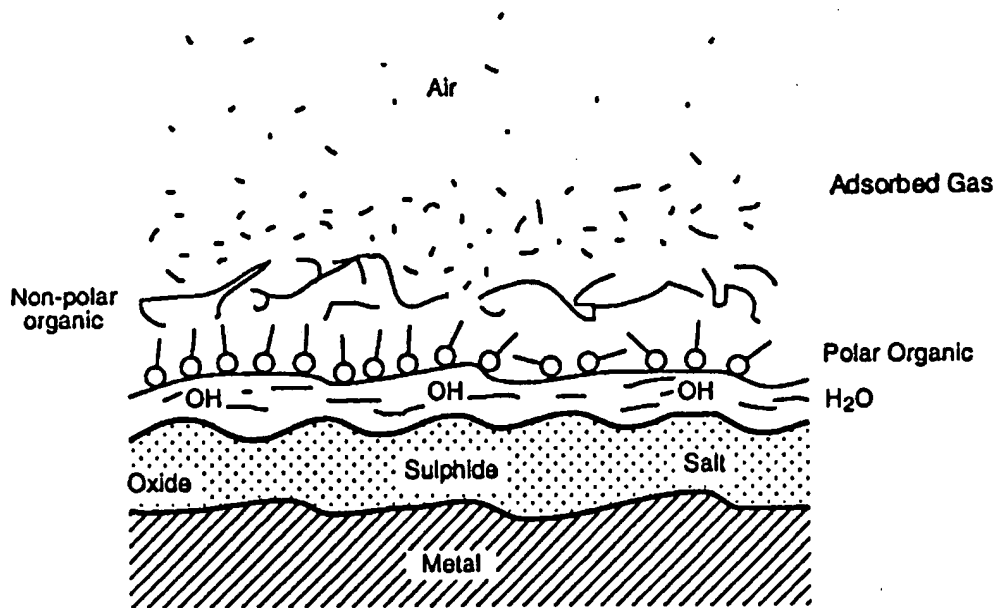
Inorganic contamination can be "brought along" with the organic residues or can be deposited independently. Inorganic residues can be



either charged (ionic) or uncharged. Ionic contaminants can be physically or chemically adsorbed. It can also be introduced into wafer subsurface layers through adsorption or by exposure to thermal energy, with resultant diffusion into the wafer.

Uncharged metallic contamination can result from replacement plating in acid etchant solutions. These contaminants are difficult to remove because they are less soluble than ions and generally require oxidation to render them soluble. The actual forces that hold contaminants on surfaces are covered in more detail in the next subsection.

A good example of a contaminated surface is shown in Fig. 1 (2). This illustration represents a typical situation on a metal surface. Many metals and semiconductors, including silicon, form thin oxide layers on the surface even under room atmospheric conditions. During this oxidation, it is possible to incorporate airborne contamination into the film. The thin "native  $\text{SiO}_2$ " on a freshly sawed silicon wafer can be contaminated with aluminum, which comes from the aluminum oxide lapping compound introduced into the room air during the lapping process (3).



**Figure 1.** An example of a contaminated metal surface (2).

## 2.1 Surface Effects—Forces Holding the Contaminants

The forces which attract and/or hold contaminants to the surface to be cleaned are multifarious in both type and extent. Although a complete discussion of these forces is beyond the scope of this chapter, a basic

understanding will help in determining how the contaminants can best be removed. The forces holding an adsorbed contaminant on the surface can be divided into two classes, depending on whether the forces are chemical or physical in character.

## 2.2 Chemical Adsorption

Chemical adsorption, or chemisorption, involves the formation of a chemical bond between the surface (adsorbent) and the contaminant (adsorbate). Chemical bonds can further be classified as *ionic*, *covalent*, or *metallic*. An ionic bond is formed when an electron is completely transferred from one atom to another, creating a positive ion and a negative ion. These ions are then held together by a coulombic force. An example of a compound of this type is NaCl. In a covalent bond, there is no permanent transfer of electrons. Instead, electrons are shared between atoms. Examples of this type include O<sub>2</sub>, N<sub>2</sub>, H<sub>2</sub>, and Cl<sub>2</sub>. The metallic bond also involves a sharing of electrons. However, in contrast to the short range sharing associated with the covalent bond, the metallic bond involves a long range sharing in which the valence electrons of each atom are shared by all atoms in the metal crystal.

It is important to remember that chemisorption is irreversible in a thermodynamic sense. Since it is necessary to break a chemical bond, it is not possible to merely rinse off (dissolve) the contaminant with a solvent.

## 2.3 Physical Adsorption

The forces involved in physical adsorption are the van der Waals or intermolecular type. These include the following:

**Dipole-Dipole.** Asymmetrical charge distribution within polar molecules results in attractive-repulsive forces on the molecules. This is termed the dipole-dipole force. Hydrogen bonding is a special form of this type of force in which a hydrogen atom forms a "bond" with a highly electronegative atom such as oxygen.

**Dipole-induced Dipole.** A polar molecule in the vicinity of a symmetrical molecule can induce a momentary dipole in the symmetrical molecule, giving rise to dipole-induced dipole forces.

**London Dispersion Forces.** London dispersion forces are explained by Hirschfelder et al. (4) in the following way: "At any instant the electrons in molecule A have a definite configuration, so that molecule A has an instantaneous dipole moment (even if it possesses no permanent electric

moment). This instantaneous dipole in molecule A induces a dipole in molecule B. The interaction between these two dipoles results in a force of attraction between the two molecules. The dispersion force is then this instantaneous force of attraction averaged over all instantaneous configurations of the electrons in molecule A."

Physical adsorption is reversible in the thermodynamic sense. Also important for aqueous cleaning is the fact that water forms strong hydrogen bonds, which can outweigh other physical adsorption forces holding the contaminants on the surface. The approximate magnitudes of the forces discussed so far are listed in Table 1 (5).

**Table 1. Relative Strengths of Binding Forces (5)**

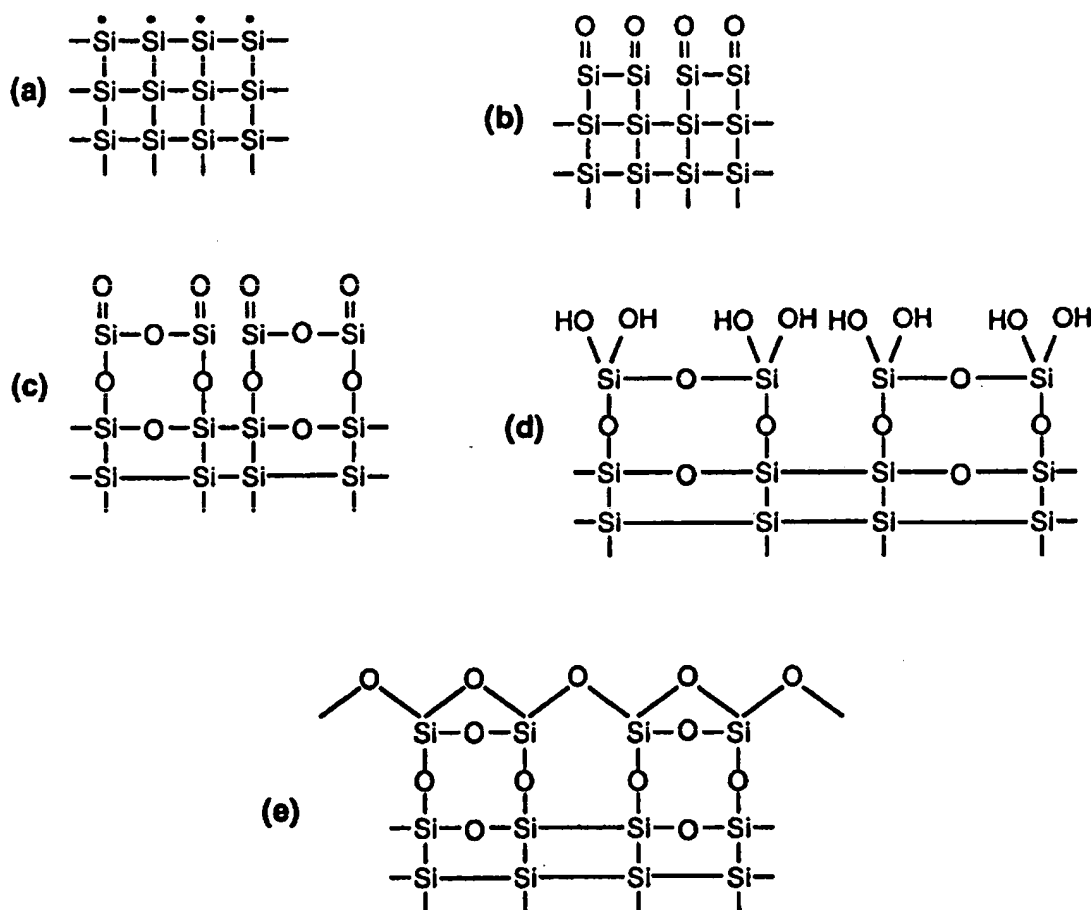
Type of Force	Energy (kcal/mol)
<b>Chemical Bonds:</b>	
Ionic	140-250
Covalent	15-170
Metallic	27- 83
<b>Intermolecular (van der Waals) forces:</b>	
Hydrogen bonds	< 12
Dipole-dipole	< 5
Dipole-induced dipole	< 0.5
Dispersion	< 10

**Other physical forces.** In addition to those already mentioned, other physical forces attract contaminants to the surface and keep them there. Gravity can deposit and hold particles on the top surface of a substrate. Electrostatic forces and the environment surrounding the surface can also be important in attracting particles.

Whitfield has shown that relative humidity can be a critical factor in surface particle retention (6). At elevated humidity levels, condensed water can fill the space between a particle and the surface. The water exerts a binding force on the particle. This phenomenon, sometimes referred to as a capillary force, increases the effect of the physical adsorption forces discussed above. To decrease the number of retained particles, it is recommended by Whitfield that surfaces not be exposed to environments

with relative humidity above 50%, even for short periods of time.

The forces which are of major importance in a particular situation are dependent on many factors. One of the most important is the chemical nature of the substrate. Not only are we concerned with its bulk composition, e.g., a silicon wafer, but also the chemical nature of the surface. In the case of a silicon wafer, the surface may be bare silicon, or oxidized silicon with a simple oxide, siloxane, silanol, or dehydrated silanol structure (See Fig. 2) (7). The exact chemical nature of the surface will determine its chemical reactivity or tendency to form chemical bonds with contaminants.



**Figure 2.** Silicon surface chemical states: (a) Bare silicon, (b) Oxidized silicon with a simple oxide, (c) Silane, (d) Silanol, (e) Dehydrated silanol (7).

Another factor is the substrate's surface texture, which may be porous, rough, or smooth on a microscale. The forces important to adsorption are short range forces. The surface texture determines how much of a particle

will come into close contact with the substrate where these forces become appreciable.

As an example of the effect of surface condition, Kern has reported that thermally steam grown  $\text{SiO}_2$  on silicon wafers retained less than  $3 \times 10^{13} \text{ Na}^+/\text{cm}^2$  after being immersed in 0.7N NaOH at  $100^\circ\text{C}$  and rinsed with water for 60 seconds. However, pyrolytically deposited  $\text{SiO}_2$ , which is more porous, retained  $1.4 \times 10^{16} \text{ Na}^+/\text{cm}^2$  after the same treatment (8).

The nature of the contaminant also determines which forces are most important. Is the contaminant a particle, an atom, a molecule or an ion? Is it organic or inorganic? What is its exact chemical makeup? Identification of the contaminant improves the chances of developing a cleaning process to successfully remove it.

### 3.0 FACTORS AFFECTING AQUEOUS CLEANING

#### 3.1 Predicting and Enhancing Contaminant Solubility

Aqueous solutions are generally polar solvents and thus are most effective in dissolving charged contaminants. The "like dissolves like" rule of thumb is used to predict the ability of a solution to dissolve a contaminant. However, relying on this principle can lead to error. For instance, because water and sugar are both rich in hydroxyl groups, water should be a good solvent for sugar, and it is. Chloroform and beryllium chloride contain about the same amount of chlorine. Chloroform could be predicted to be a solvent for this salt. In fact, beryllium chloride is insoluble in chloroform.

A better prediction of solubility is based on the solubility parameter of the two materials, solute (contaminant) and solvent (proposed cleaning solution). This solubility parameter is a measure of the "internal pressure" of a substance and can be defined as the square root of the energy of vaporization per cubic centimeter:

$$\sigma = (H_v/V)^{1/2}$$

where:  $\sigma$  = solubility parameter  
 $H_v$  = molar heat of vaporization  
 $V$  = molar volume

The solubility parameter can also be calculated from other properties, such as surface tension, van der Waals constant for a gas, critical pressure,

and air viscosity. Regardless of the calculation procedure used, when the values of the solute and solvent solubility parameters are close, the likelihood of high solubility increases (9)(10).

The solubility of a contaminant can be increased by modifying one or more of several parameters, such as concentration, pH, temperature, or by the addition of another solution component. Process parameters such as these are discussed in more detail in Sec. 6. Another method of improving the solubility of contaminants is the formation of soluble complexes. Many metal ions can be made more soluble this way. Thus, the anion used in an acid solution can be important, since it may contribute to complex formation. The metal ion acts as an electron acceptor (Lewis acid) and the solution anion acts as the electron donor (Lewis base), or "ligand", in the formation of an inorganic complex or coordination compound. For example, when copper is to be removed, nitric acid is a better choice than hydrochloric acid, possibly because nitrate ( $\text{NO}_3^-$ ) is a better ligand for copper than chloride ( $\text{Cl}^-$ ). Change in acidity alone cannot explain this effect, since hydrochloric acid and nitric acid are similar in strength.

The ability of negative ions to form complexes or coordination compounds can be ranked. As seen in the example with copper,  $\text{Cl}^-$  ranks below  $\text{NO}_3^-$ . Although both  $\text{NO}_3^-$  and  $\text{NO}_2^-$  are present in nitric acid solutions, complexes will form predominantly with  $\text{NO}_2^-$ . The negative ion ligand preference series tends to rate relative base strength and corresponding preference as a ligand (11):



Contaminants may be made more soluble, and thus removable, by allowing a solution component to react with the contaminant to form a more soluble species. This is a very prominent mechanism in organic removal, where the insoluble material is oxidized to a more soluble species such as a carboxylic acid. In order to take advantage of this phenomenon, an oxidizing agent, such as hydrogen peroxide, ammonium persulfate, or ozone can be added to the solution. Also, a strong oxidizing acid, such as nitric acid, could be used.

### 3.2 Etching as a Means of Contaminant Removal

A contaminant which is partly absorbed into the subsurface of a wafer can be very difficult to remove with cleaning agents. For example, sodium

ions can be "trapped" when the base silicon surface forms a native oxide in an environment containing sodium. Furthermore, surface sodium ions can migrate through the oxide during a high temperature operation.

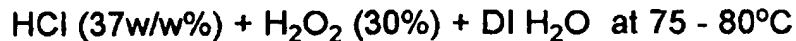
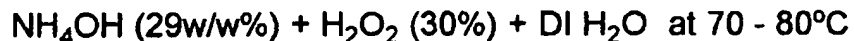
Removal of a subsurface contaminant can be facilitated by a light surface etch which carries off some of the contaminant in the process. In the case of removing a surface oxide, any contaminants left after the etching process may now reside at the surface and thus are much easier for the cleaning solutions to remove.

Another instance in which etching is useful is for the removal of silicon particles. When initially deposited, the particles can be removed by rinsing with water, particularly if a wetting agent is added. However, if allowed to dry, both the silicon surface and the particles begin to oxidize. It is likely that this oxidation leads to an intermingling, and the two oxides become interlocked (12). Besides physical means, etching appears to be the only effective way of removing these particles.

### 4.0 CLEANING CHEMISTRIES

Many chemical solutions have been used for cleaning wafers. The most prevalent have been the RCA solutions, aqueous mixtures of unstabilized hydrogen peroxide with ammonia and hydrochloric acid. These cleans were developed before 1970 and have been the primary cleaning method used by the industry ever since (8)(13)(14).

The original RCA clean consisted of two cleaning solutions:



The purpose of the first step, known as Standard Clean 1 or SC-1, was to oxidize surface organic films and remove some metal ions. The second step, known as Standard Clean 2 or SC-2, was to remove alkali cations and other cations like  $\text{Al}^{+3}$ ,  $\text{Fe}^{+3}$  and  $\text{Mg}^{+2}$ . The solutions were mixed typically in the ratio 1:1:5.

The RCA cleaning chemistries, as well as other cleaning solutions, are listed in Table 2. The ratios of the chemicals have been omitted since they can vary greatly between fabs. The solutions listed in Part 2 of Table 2 have been reported only recently.

**Table 2. Silicon Wafer Cleaning Solutions**

Solution	Chemical Symbols	Common Name	Purpose or Removal of:
<b>Part 1.</b>			
Ammonium hydroxide/ hydrogen peroxide/ water	$\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$	RCA-1, SC-1 (Standard Clean-1), APM (ammonia/peroxide mix), Huang A	Light organics, particles, and metals; protective oxide regrowth (14)
Hydrochloric acid/ hydrogen peroxide/ water	$\text{HCl}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$	RCA-2, SC-2 (Standard Clean-2), HPM (hydrochloric/peroxide mix), Huang B	Heavy metals, alkalis, and metal hydroxides (14)
Sulfuric acid/ hydrogen peroxide	$\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$	Piranha, SPM (sulfuric/peroxide mix), "Caros acid"	Heavy organics (15)
Hydrofluoric acid/water	$\text{HF}/\text{H}_2\text{O}$	HF, DHF (dilute HF)	Silicon oxide
Hydrofluoric acid/ ammonium fluoride/ water	$\text{HF}/\text{NH}_4\text{F}/\text{H}_2\text{O}$	BOE (buffered oxide etch), BHF (buffered hydrofluoric acid)	Silicon oxide
Nitric acid	$\text{HNO}_3$		Organics and heavy metals
Choline	$(\text{CH}_3)_3\text{N}^+ \cdot \text{CH}_2\text{CH}_2\text{OH} \cdot \text{OH}^-$	trimethyl(2-hydroxyethyl) ammonium hydroxide	Metals and organics (16)
Choline/ hydrogen peroxide/water	$(\text{CH}_3)_3\text{N}^+ \cdot \text{CH}_2\text{CH}_2\text{OH} \cdot \text{OH}^- / \text{H}_2\text{O}_2/\text{H}_2\text{O}$	Choline/ peroxide	Heavy metals, organics and particles (16)
Ammonium persulfate/ sulfuric acid	$(\text{NH}_4)_2\text{SO}_4/\text{H}_2\text{SO}_4$	SA-80	Organics (17)
<b>Part 2. Silicon Wafer Cleaning Solutions Developed Since 1987</b>			
Peroxydisulfuric acid/sulfuric acid	$\text{H}_2\text{S}_2\text{O}_8/\text{H}_2\text{SO}_4$	PDSA, "Caros acid," Piranha	Organics (18)
Ozone dissolved in deionized water	$\text{O}_3/\text{H}_2\text{O}$	Ozonized water	Protective oxide regrowth; organics (19)
Sulfuric acid/ozonized water	$\text{H}_2\text{SO}_4/\text{O}_3/\text{H}_2\text{O}$	SOM (sulfuric/ozone mix)	Organics (19)
Hydrofluoric acid/ nitric acid	$\text{HF}/\text{HNO}_3$		Slight Si etch; metals (20)
Hydrofluoric acid/ hydrogen peroxide	$\text{HF}/\text{H}_2\text{O}_2$		Slight Si etch; metal (21)



## **5.0 AN EXAMPLE OF AN AQUEOUS CHEMICAL CLEANING PROCESS**

The sequence of chemical solutions used to clean a wafer depends upon the contaminants present and the requirements of the clean. A general discussion of the effects of chemical sequence is beyond the scope of this chapter. Possible sequences of the chemistries used in a common modified RCA clean will be discussed as an example. This clean, which can be used to remove most contaminants, consists of the following steps:

- Organic removal
- Native oxide removal
- Particle removal with simultaneous oxide regrowth
- Metal removal

### **5.1 Organic Removal**

Organic removal is often the first step in cleaning because the presence of organic films on wafer surfaces can render the surface hydrophobic and prevent other cleaning solutions from reaching the surface. Two solutions are commonly used for removing organic films. If heavy organic contamination like photoresist is present, mixtures of  $\text{H}_2\text{SO}_4$  and  $\text{H}_2\text{O}_2$  at temperatures  $>100^\circ\text{C}$  are often used (15). Light organics can be removed at  $80^\circ\text{C}$  using the  $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$  chemistries described above (13). If very heavy contamination is present the  $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$  solution followed by the  $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$  solution may be effective.

### **5.2 Native Oxide Removal**

The native oxide removal step is included because a thin layer of oxide is always present on a silicon surface and inorganic contaminants are often trapped in this layer. When the oxide is removed the contaminants are also removed, resulting in a surface with very low metallic contamination (12).

Oxide can be removed using either dilute solutions of HF or buffered oxide etch (BOE). BOEs are used instead of dilute HF because they provide a more stable etch rate and prevent photoresist liftoff which can occur in dilute HF. However, the formulation of BOEs is not straightforward. Surfactants are often added to improve wetting of the wafer surface since silicon becomes hydrophobic when the oxide is removed. The surfactants tend to make the solution foam, so defoamers are added. Optimization of this multicomponent solution is a very complex task (22).

HF solutions need to have extremely low metal levels to be effective. Metals like copper and gold, which have a lower electronegativity than silicon, can plate onto the wafer surface (23)(24). The solutions should also be free of organics, as should all subsequent cleaning or rinsing solutions used before a clean oxide is grown, because the hydrophobic silicon surface is very prone to hydrocarbon adsorption (25). In addition, the hydrophobic surface following this clean is very susceptible to particulate contamination (26)(27) that may result when it is exposed to gas-liquid interfaces (25). Hence, the methods used to rinse and dry the wafer following this step are critical in controlling particle contamination (28).

### 5.3 Particle Removal With Simultaneous Oxide Regrowth

Because the oxide removal process tends to add particles to the wafer surface, it is often followed by an  $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$  step. This step is effective in both removing particles and growing a thin oxide film. The oxide "passivates" the surface by making it hydrophilic and less susceptible to organic and particulate contamination (29)(30). Particles are presumably removed by slowly etching the surface of the silicon from under the particles. The etch rate is a function of the type of oxide present and is in the range of 0.09 - 0.4 nm/min at 80°C when the ratio of  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  is 1:1:5 (31). This step is extremely effective in removing particles when it is combined with sonic cleaning (32). The use of sonic cleaning for particle removal is discussed in more detail in Sec. 8.4.

One disadvantage of using the  $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$  solution to grow an oxide is that some metals are insoluble in this highly basic solution and, if present, have a high tendency to precipitate onto the wafer surface. Aluminum is an example of a metal of this type which, when present in sub-ppm concentrations can cause a substantial shift in the flat band voltage of a dual dielectric (33). Also, because aluminum is one of the few metals which does not cause  $\text{H}_2\text{O}_2$  to decompose, the equipment used to make and store  $\text{H}_2\text{O}_2$  was historically made of aluminum. The resulting  $\text{H}_2\text{O}_2$  contained significant levels of aluminum (34). Recent advances in the technology of making  $\text{H}_2\text{O}_2$  have virtually eliminated this source of contamination (35).

### 5.4 Metal Removal

Metal removal is usually accomplished using the  $\text{HCl}/\text{H}_2\text{O}_2$  solution described above. This solution effectively removes metals and prevents

them from plating back onto the surface by complex formation. It has been shown to be effective for removing cobalt, copper, iron, lead, magnesium, nickel and sodium as well as aluminum precipitated from the  $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$  solutions (14) and other metals.

## **6.0 EFFECTS OF PROCESS VARIABLES ON AQUEOUS CHEMICAL CLEANING**

The material presented so far in this chapter has noted that many aqueous chemistries are available for cleaning wafers. Their effectiveness in providing a contamination-free surface depends upon a number of variables, including the sequence of chemistries used, the ratio of the chemicals, the processing temperature, the age of the solutions, etc. Hence, aqueous cleaning is a complex process which often must be tailored to specific needs. For example, the structure and growth rate of oxides is highly dependent upon the cleaning procedures used to prepare the surface prior to oxide growth (36)-(38). This section describes the effects of some of these variables on wafer surface properties.

### **6.1 The Effect of Changing the Sequence of the Chemical Cleaning Steps**

The four-step cleaning sequence described in Sec. 5 results in a silicon surface with low metal, organic and particle contaminant levels and a thin layer of chemical oxide. If the oxide removal step is eliminated, the metal levels following the complete clean are higher, as shown in Table 3 (39). The purpose of the HF is to remove small amounts of surface oxide, which improves removal of inorganic species. This suggests that the HF acts by a surface etching mechanism. When the order of the HF and  $\text{NH}_4\text{OH}$  steps are switched, metal levels are reduced. However, particle levels are increased by approximately a factor of four.

Because the wafer surface following native oxide removal has very low metal levels, it has been considered for a final step in cleaning. However, its use did not become practical as a final step until recently because of the contamination issues associated with particles, organics and metals. Improvements in the purity of HF solutions and in the quality of the water used to rinse the surface following the cleaning step has made its use practical (40)(41). This clean is now capable of producing surfaces with very low metal levels and low particle counts, as shown in Table 4.

**Table 3.** The Effect of Cleaning of Silicon Wafers With and Without HF Solution on Metallic Contamination (39)

Cleaning Sequence	SIMS Result (metal/Si x 10 <sup>-9</sup> )		
	Na	K	Cu
Complete*	26	156	233
Without HF**	90	246	658

\* Cleaning sequence was:

96% H<sub>2</sub>SO<sub>4</sub>:30% H<sub>2</sub>O<sub>2</sub> (4:1)

0.5% HF

29% NH<sub>4</sub>OH:30% H<sub>2</sub>O<sub>2</sub>:DI water (1:1:5)

37% HCl:30% H<sub>2</sub>O<sub>2</sub>:DI water (1:1:5)

\*\* Cleaning sequence was:

96% H<sub>2</sub>SO<sub>4</sub>:30% H<sub>2</sub>O<sub>2</sub> (4:1)

29% NH<sub>4</sub>OH:30% H<sub>2</sub>O<sub>2</sub>:DI water (1:1:5)

37% HCl:30% H<sub>2</sub>O<sub>2</sub>:DI water (1:1:5)

**Table 4.** Metal Contamination on Silicon Wafer Surfaces After Oxide Removal in an HF-Last Clean (40)

Metal	Concentration (atoms/cm <sup>2</sup> )
Cr	< 2 x 10 <sup>10</sup>
Fe	< 2-3 x 10 <sup>10</sup>
Ni	< 2-4 x 10 <sup>10</sup>
Cu	10-45 x 10 <sup>10</sup>
Zn	< 2 x 10 <sup>10</sup>

If HCl is added to the HF solution in this "HF-last" clean, still lower metal levels can be achieved. The chloride ion forms complexes with many metals as described in Sec. 3.1, thereby reducing plate back, as shown in Table 5 (42).

Ozonized water can be used instead of the NH<sub>4</sub>OH/H<sub>2</sub>O<sub>2</sub> to control growth of a protective oxide layer following the oxide strip (19)(42). Ozone has an oxidation potential similar to that of H<sub>2</sub>O<sub>2</sub> and can be used to grow

a very clean oxide. Unlike the  $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$  step, ozonization does not remove particles. However, if the wafer is handled properly after the oxide is stripped, particle removal is not necessary. In addition, because this treatment results in a surface with lower metal content than the modified RCA clean described above, the HCl-based metal removal step is not required, as shown in Table 6 (19).

**Table 5.** The Effect of HCl Addition into an HF Oxide Stripping Solution on Metallic Contamination on Silicon Wafer Surfaces (42)

Stripping Solution	SIMS Relative Element Concentration					
	Na	K	Al	Ca	Mg	Fe
10% HF	6	10	7	60	8	7
10% HF + HCl*	1	10	1	10	4	2

\* Concentration not defined in reference.

**Table 6.** The Effect of Ozone Oxide Growth on Metallic Contamination (19)

Cleaning Sequence	SIMS Relative Element Concentration				
	Na	K	Cu	Ca	Mg
Modified RCA*	22	6	<2	11	2
Ozone Oxide Growth**	10	2	<2	10	1

\* Cleaning sequence was:

96%  $\text{H}_2\text{SO}_4$ :30%  $\text{H}_2\text{O}_2$  (4:1)

0.5% HF

29%  $\text{NH}_4\text{OH}$ :30%  $\text{H}_2\text{O}_2$ :DI water (1:1:5)

37% HCl:30%  $\text{H}_2\text{O}_2$ :DI water (1:1:5)

\*\* Cleaning sequence was:

96%  $\text{H}_2\text{SO}_4$ :Ozonized water

0.5% HF

Ozonized water

Another method of removing and regrowing the thin native oxide is through the controlled etch method. In this technique chemicals which etch and oxidize silicon are combined. These two competing reactions slowly etch the surface and form a new oxide layer without exposing a hydrophobic surface. Two solutions have been used to achieve controlled etch: mixtures of HF/HNO<sub>3</sub> and mixtures of HF/H<sub>2</sub>O<sub>2</sub> (43). Both are very effective in producing surfaces with low metal contamination.

## 6.2 The Effect of Concentration

The concentrations of reactants in the chemical solutions used to clean wafers can significantly alter the effectiveness of the solution in creating a contaminant-free silicon surface. For example, it was originally thought that the ratios in the NH<sub>4</sub>OH/H<sub>2</sub>O<sub>2</sub>/water (SC-1) clean were not very important. Subsequent studies have revealed that if the ratio of NH<sub>4</sub>OH to H<sub>2</sub>O<sub>2</sub> is too high the wafer will be etched (44). Another study indicated that the amount of NH<sub>4</sub>OH should be substantially reduced to increase the removal efficiency of small particles and to prevent formation of surface microroughness (45). In this study a ratio of 0.05:1:5 was recommended. However, this study did not address the removal of microcontaminant films which might require higher concentrations (14).

The etchant to oxidizer ratio used in controlled etch cleans is very important. If the amount of etchant is too high the surface is roughened and device electrical properties are affected. If the etchant concentration is too low the metal impurities in the original native oxide are not removed.

The concentration of HF used for oxide removal also plays a role in the effectiveness of cleans performed. Decreasing the HF concentration decreases the ratio of F-terminated to H-terminated silicon atoms on the wafer surface. The decreased F concentration reduces the rate at which oxide grows on the silicon wafer surface when it is exposed to either water or air (46).

## 6.3 The Effect of Temperature

Changing the temperature of a cleaning solution can have several important effects:

1. Increasing the temperature increases the rate of reactions. A rough rule of thumb is that an increase of 10°C doubles the reaction rate. This rule applies to both desired reactions and undesired side reactions.

2. Increasing the temperature usually increases the solubility of contaminants and reaction products. Table 7 lists the relative solubility of various metal salts as a function of solution temperature (11). Some contaminants (Group A) become considerably more soluble as the water temperature is increased (e.g.,  $\text{FeSO}_4$ ,  $\text{NH}_4\text{HCO}_3$ ). However, Group B chemicals (e.g., sodium chloride) show very little increase in solubility with increasing water temperature and Group C compounds actually decrease in solubility with increased temperature. Therefore, knowledge of the solute and the solvent are necessary to select the best conditions to promote solubility. When the solubility increases, the cleaning rate increases.
3. Increasing the temperature can increase the rate and probability of contaminants plating onto the wafer surface.
4. Increasing the temperature increases the decomposition rate of unstable reactants. For example,  $\text{H}_2\text{O}_2$  decomposes to form water and oxygen. The rate of decomposition approximately doubles with every  $10^\circ\text{C}$  increase.

Although higher temperatures are preferred, it is often necessary to make tradeoffs. For example, the  $80^\circ\text{C}$  temperatures normally used for the SC-1 and SC-2 cleans was chosen to maximize the cleaning effectiveness without decomposing the  $\text{H}_2\text{O}_2$  too rapidly (14).

The manufacturers of commercially available chemical blends often recommend specific temperature ranges that give optimal performance. If the recommended temperature ranges are not used, cleaning may be inadequate or may require significantly longer than expected.

## 6.4 Wetting

Chemicals must wet a surface before they can clean it. The wettability of a solid surface depends upon the surface tension of both the solid and the solution. When the surface tension of the solid is greater than or equal to the surface tension of the solution it wets. If it is lower it does not wet. Many common organic solvents have surface tensions which are lower than water. Many inorganic solutions have surface tensions which are greater than water.

The surface tension of a wafer surface is a function of its chemical nature. Surfaces with a native oxide are hydrophilic (wet with water), whereas those with no oxide are hydrophobic (do not wet with water). In addition, the presence of contaminants on the wafer surface can change its

surface tension. Organic contaminants in particular can drastically decrease the surface tension of a hydrophilic wafer surface rendering it hydrophobic.

**Table 7. Solubilities of Inorganic Compounds in Water at Various Temperatures (11)**

Substance	Formula	0°C	20°C	40°C	60°C	80°C	100°C
<b>GROUP A</b>							
Ammonium oxalate	$(\text{NH}_4)_2\text{C}_2\text{O}_4$	2.2	4.4	8.0	---	---	---
Ferrous sulfate	$\text{FeSO}_4$	15.65	26.5	40.2	---	---	---
Ammonium bicarbonate	$\text{NH}_4\text{HCO}_3$	11.9	75.5	91.1	107.8	126	145.6
Potassium chloride	KCl	27.6	34.0	40.0	45.5	51.1	56.7
Calcium chloride	$\text{CaCl}_2$	59.5	---	---	136.8	147.0	159
Cupric chloride	$\text{CuCl}_2$	70.7	77.0	83.8	91.2	99.2	107.9
Sodium nitrate	$\text{NaNO}_3$	73	88	104	124	148	180
Potassium iodide	KI	127.5	144	160	176	192	208
Ammonium manganese phosphate	$\text{NH}_4\text{MnPO}_4$	---	192	297.0	421.0	580.0	871.0
Calcium iodate	$\text{Ca}(\text{IO}_3)_2$	---	208.8	242.5	284.6	354.5	426.3
Zinc iodide	$\text{ZnI}_2$	429.4	---	445.2	467.2	490	510.5
<b>GROUP B</b>							
Sodium chloride	NaCl	35.7	36.0	36.6	37.3	38.4	39.8
<b>GROUP C</b>							
Sodium carbonate	$\text{Na}_2\text{CO}_3$	---	---	48.5	46.4	45.8	45.5
Calcium sulfate	$\text{CaSO}_4$	0.1759	0.1688	0.0973	0.0576	---	0

Group A - Solubility increases as temperature increases.  
Group B - Solubility shows no change as temperature increases.  
Group C - Solubility decreases as temperature increases.

Wetting agents, or surfactants, are sometimes added to cleaning solutions to promote wetting. These surface active agents reduce the interfacial tension between the solution and the wafer surface, allowing the solution to spread evenly across the wafer. The effectiveness of a surfactant to promote wetting is a function of its structure (47).



**6.5 The Effect of Solution Degradation**

There are several effects besides reactant decomposition which can cause solution cleaning effectiveness to change with time.

**Reactant Depletion.** Most of the reactions that remove contaminants from wafer surfaces reduce the concentration in the solution as the reaction takes place. A decrease in concentration usually results in a decrease in reaction rate. The rate of change in concentration is usually very slow unless large amounts of contaminants need to be removed. However, if the concentration of reactant is low, the contaminant concentration is high and the solution is used to process many wafers, the change in reactant concentration can result in a decrease in the reaction rate. A dilute HF bath is an example of a solution in which this might occur.

**Solution Contamination.** The function of cleaning solutions is to remove contaminants. When contaminants are removed from wafers they are sometimes converted into harmless byproducts. However, in many cases contaminants are simply removed from the wafer surface and remain in an active form in the cleaning solution. In this case, the concentration of contaminants in the solution increases as additional wafers are processed. Eventually, the concentration can increase to the point where the bath can contaminate subsequent wafers. Hence, the bath must be replenished or the contaminants must be removed before their concentrations reach unacceptable levels.

**Component Removal.** Many of the chemical cleaning processes described above are performed in recirculated baths in which filtration is employed to remove particles generated in the cleaning process. Unfortunately, filters can sometimes remove components from the cleaning solution. For example, some surfactants added to oxide etchants to enhance wetting are removed by adsorption (48). Filtration cannot be used unless the filter is compatible with all components in the solution.

**CO<sub>2</sub> Absorption.** Some of the solutions used to clean semiconductor wafers are basic. These solution can absorb CO<sub>2</sub> from the atmosphere. The CO<sub>2</sub> forms carbonic acid which reacts with the bases present in the solution, thereby decreasing the solution strength. Although the change in concentration is fairly slow, it can change the solution effectiveness if the bath is not changed frequently. Absorption can be prevented by blanketing the bath with an inert gas like nitrogen or argon.

**Evaporation.** Chemical solutions exposed to the atmosphere can release volatile components. This release results in changes in the chemical properties of the bath, thereby changing cleaning effectiveness.

Since evaporation increases exponentially with temperature, this effect is more pronounced at higher temperatures.

## 6.6 Carrier Effects

Wafers are often cleaned in batches of twenty-five or fifty or more. When cleaning is performed in this manner a carrier is required to hold the wafers. The carrier must be made of material that is compatible with the cleaning solutions to which it will be exposed. Carriers are often made of Teflon\* because of its excellent chemical resistance. However, Teflon is somewhat porous and can absorb tangible amounts of chemicals (49) that can be carried to subsequent processes, resulting in contamination. In addition, some grades of Teflon slowly outgas trace amounts of HF that can etch oxide-coated wafer surfaces (50). Hence, care must be taken to ensure that the carriers used do not contribute to contamination; they should be frequently cleaned to remove absorbed impurities.

## 7.0 SEMICONDUCTOR WAFER DRYING

Much attention has been given to the wafer cleaning process, but the drying of the clean wafers is equally critical. In fact, wafer drying may be the most important step for ensuring that a cleaning process is successful in eliminating contamination. The drying process must remove water from the surface before it can evaporate, leaving residue behind (14)(51). There are three basic drying mechanisms: physical separation as in centrifugal drying, solvent displacement of DI water followed by solvent removal as in vapor drying, and evaporation as in hot water drying techniques.

### 7.1 Centrifugal Drying

Centrifugal or spin dryers are very common in the semiconductor industry. The centrifugal force resulting from spinning wafers at high speed eliminates the major portion of water from the wafer surface. The thin layer left behind evaporates. Because the evaporating water layer is very thin, deposition of residuals is minimal (52).

Two types of drying equipment are commonly used: horizontal and downflow. In horizontal systems wafer cassettes are inserted with the

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\* Teflon is a registered trademark of E. I. DuPont de Nemours, Wilmington, Delaware.

wafers oriented vertically. In downflow dryers the wafers are positioned horizontally. A diagram of a downflow dryer is shown in Fig. 3 (52). In downflow dryers water is removed both by centrifugal force and by air which is drawn across the wafer surface by the rotating action.

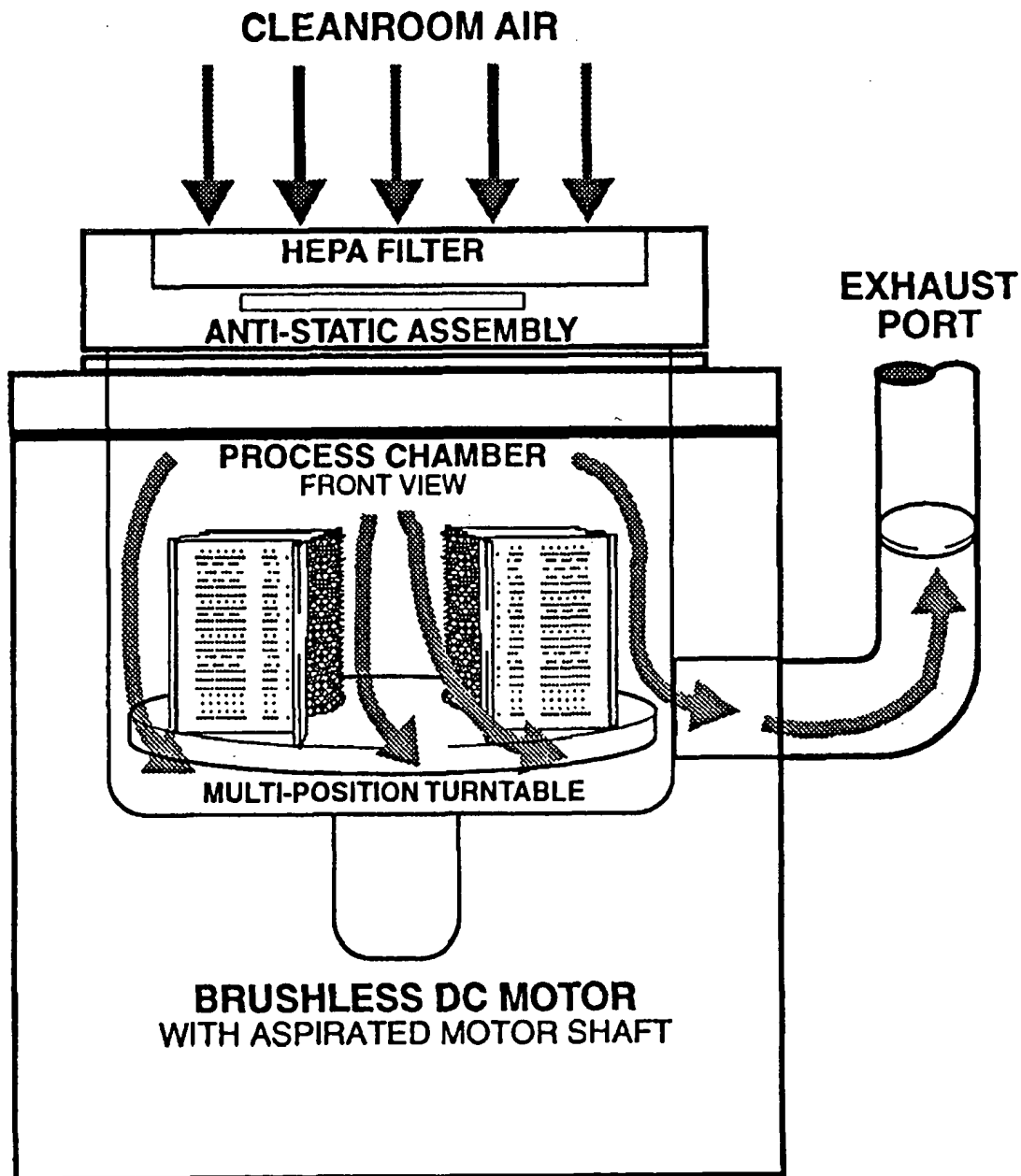
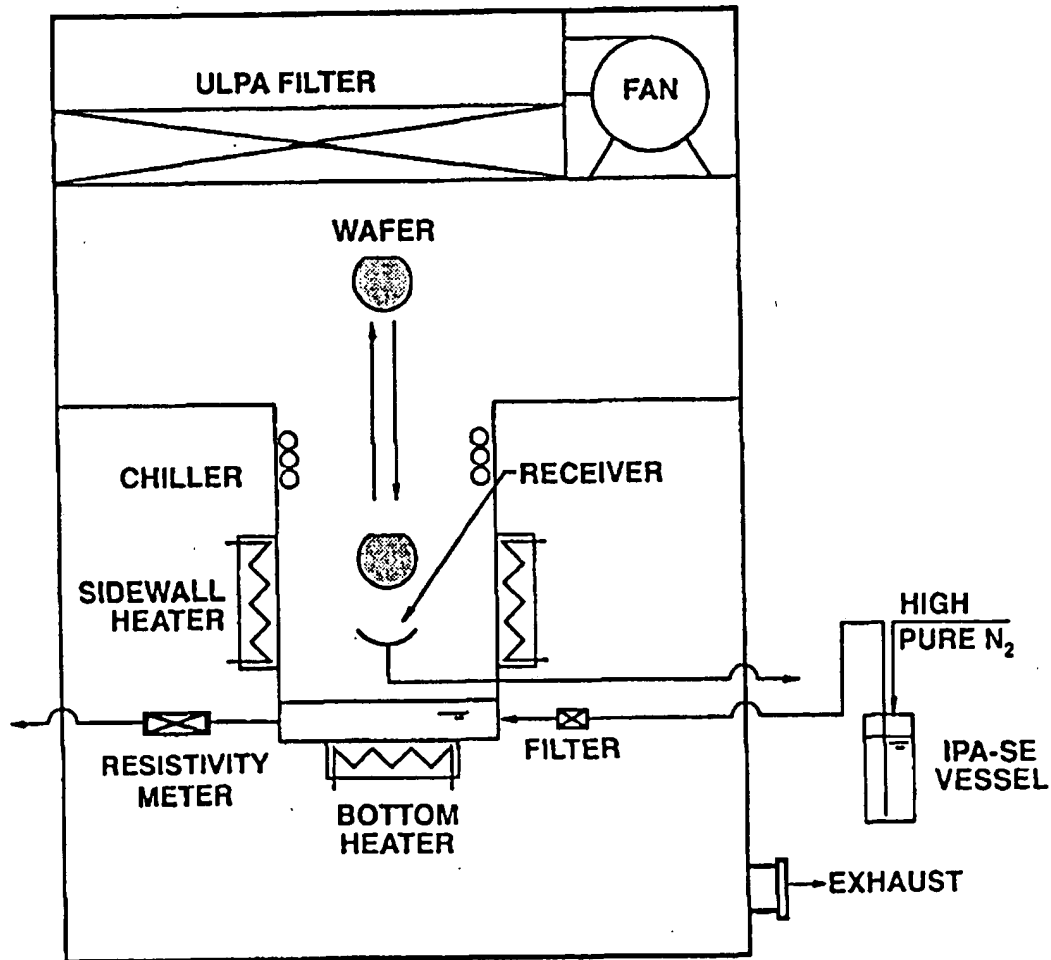


Figure 3. Cross section of a downflow centrifugal dryer (52).

## 7.2 Vapor Drying

In vapor drying, wafers wet with deionized water are suspended in a solvent vapor emanating from a heated bath. The vapor displaces the water on the wafer, leaving a vapor "coated" surface. When displacement is complete, wafers are raised above the vapor cloud and dry very quickly due to the high volatility of the solvent (53)(54). Vapor dryers are attractive because they eliminate some of the problems associated with spinning wafers, however, acceptance has been slow. In part this is due to concern over potential organic residues and safety problems (3). A schematic diagram of a vapor dryer is shown in Fig. 4 (55).



**Figure 4.** Cross section of an isopropyl alcohol vapor dryer (55). (Copyright 1989, IEEE)

The solvent used in vapor dryers has been primarily isopropyl alcohol (IPA). Mixtures of other solvents are under investigation but are not yet commercially available. The solvents being investigated usually have high flash points, thus offering greater safety than IPA.

The design of the vapor dryer has been hampered by the thermal mass of the carrier and platform, especially for larger wafers. When introduced into the hot vapor zone from the room ambient temperature, the large thermal mass can cause the vapor cloud to collapse. The result is ineffective drying, water evaporation from the wafers, and greater residuals (particles, etc.) on the wafer surface.

### **7.3 Hot Water Drying Techniques**

A drying system based on the surface tension and capillary action of water is illustrated in Fig. 5 (56). In this technique, sometimes termed slow pull drying, wafers in a cassette are immersed into a tank of hot DI water where rinsing takes place. When rinsing is complete, the wafers are lifted slowly and at a controlled velocity from the bath. Because the wafers are pulled slowly and constantly, the water is not broken into droplets. Capillary action and surface tension pull the deionized water from the surface of wafers back into the bath. The wafers are dry once the cassette is removed. Although the technique's advantages of minimal stress on the wafer and simplicity of the tool's mechanisms are recognized, the technique has not yet been widely accepted (51).

## **8.0 EQUIPMENT USED FOR AQUEOUS CLEANING**

### **8.1 General Design Considerations**

The equipment used for cleaning semiconductor wafers must be capable of supplying a number of chemicals and chemical mixtures to the wafer surface in a defined sequence. The equipment must provide for rinsing between chemicals to prevent cross contamination. Also, drying capabilities must be included.

High-purity chemicals are required for cleaning because the wafers are very susceptible to damage by contamination. Hence, the materials of construction used in the equipment must be compatible with the chemicals and selected to minimize the equipment as a source of contamination.

Parts that contact liquids must be free of dead spots where contamination or bacteria may collect. Materials must be carefully selected to avoid chemical leaching and flaking.

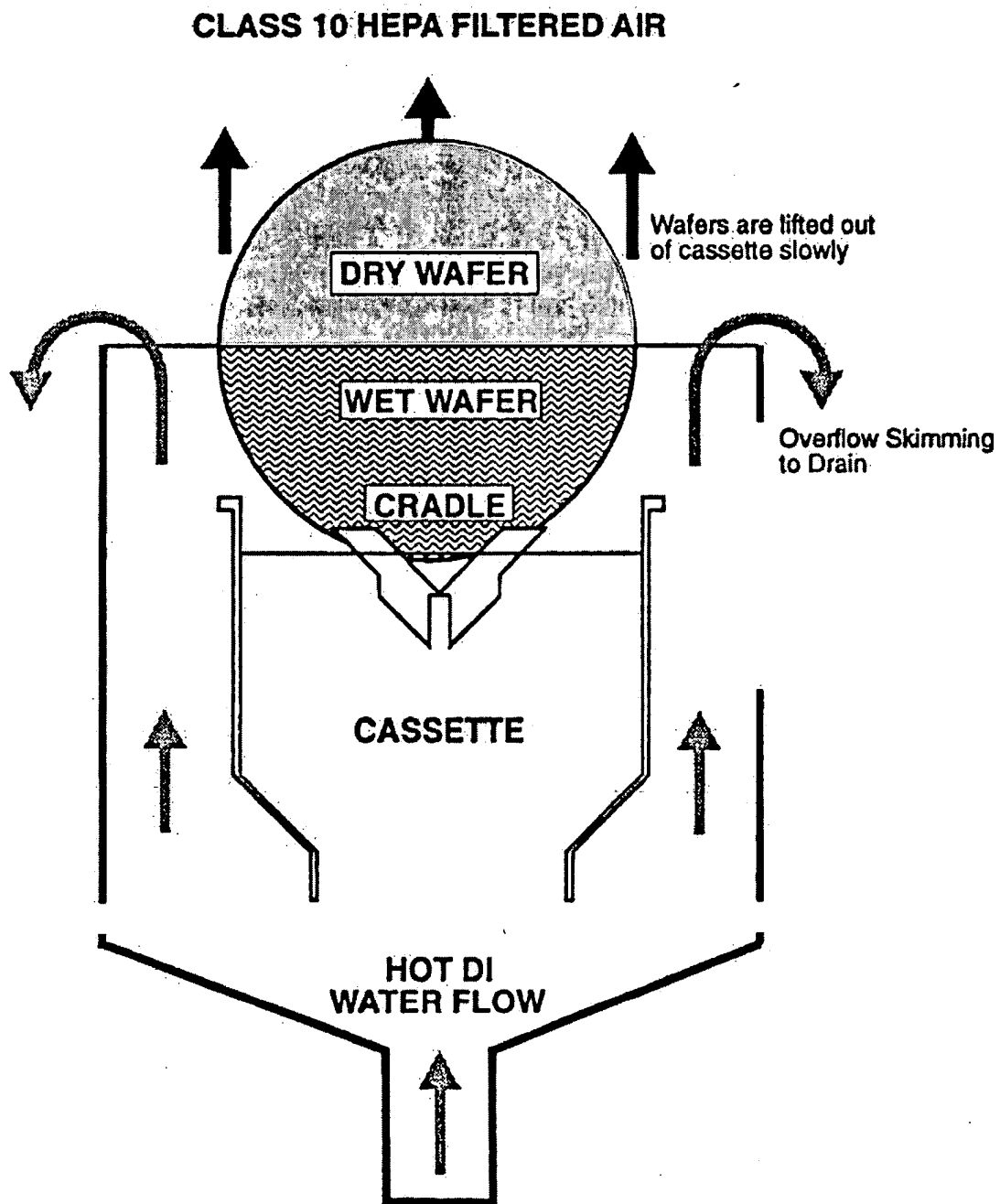


Figure 5. Slow pull dryer (56).

Contamination resulting from a poor choice of materials may be relatively obvious or fairly subtle. A more subtle example would be low levels of boron contamination which can originate from Pyrex and deposit on semiconductor wafer surfaces. Boron can cause electrical anomalies in the final chip if the contamination is high enough or occurs in a sensitive area of the device.

Metal leaching from stainless steel can also occur. The alkaline and acidic chemicals used in cleaning are highly corrosive. Although stainless steels are relatively corrosion resistant, they are not corrosion proof. They are formulated to slow the rate of attack, but they do not completely stop it. Corrosive solutions coming into contact with these surfaces will pick up Fe, Ni, and Cr, as well as other metals used in their manufacture. Even ultrapure water will dissolve stainless steel to the extent that 18 megohm-cm water will degrade to unacceptable levels after a brief exposure.

A very common set of materials used in construction of wet cleaning equipment is the Teflon family of fluorinated polymers and other polyfluorocarbons. These materials are used because of their extensive chemical resistance. Teflon polytetrafluoroethylene (PTFE) is a white, opaque material which must be shaped initially by techniques similar to those of powder metallurgy. Teflon fluorinated ethylenepropylene (FEP) and Teflon perfluoroalkoxy (PFA) are melt-processable resins with significantly improved ease of fabrication compared with that of PTFE.

The high chemical resistance of Teflon polymers to semiconductor cleaning chemicals helps make Teflon the chosen material for many processes. Chemical resistance can be estimated by measuring the absorption of chemicals by the material. Although Teflon absorptivities are unusually low compared to other plastics or elastomers, fluoride ions and related compounds are absorbed into the resins. Absorption is a function of temperature and pressure. Prolonged retention of absorbed chemicals can result in their decomposition within the Teflon matrix. Since the exposure time is long in some applications, it is advisable to perform in-process testing to ensure that the Teflon properties have not been altered (57)(58).

## **8.2 Immersion Processors**

Immersion processors, or wet benches, are based on the principle that wafers are immersed sequentially into the proper chemical solutions in separate baths. In a typical wet bench clean operation, a cassette of wafers is immersed in an appropriate solution for a specified period of time, after which it is rinsed in DI water. The rinse terminates the reaction. The

cassette of wafers is similarly immersed in subsequent cleaning and rinsing solutions. After a final rinse with filtered DI water, the wafers are dried. The original RCA cleaning process was developed in a simple immersion system of this type (13)(52). An example of a bench system using immersion processing is shown in Fig. 6 (59).

Many cleaning processes are performed at elevated temperatures. Immersion baths can be directly or indirectly heated to achieve the desired temperature. Physical agitation is used often to flush away contaminants and provide fresh solutions to the surface being cleaned. The agitation is accomplished in various ways including ultrasonic agitation (described in Sec. 8.4), nitrogen bubbling through the solution, or mechanical movement of the part in the solution.

Several recent developments in wet bench technology have substantially improved its performance. Automated wet benches with robotics handling have been introduced over the last five years. Although this type of system is considerably more expensive than manual units, it has gained acceptance in many fabs. Filtered recirculation of chemicals has been employed to improve chemical cleanliness and reduce chemical consumption. In the past, the use of circulation systems had been limited to lower temperatures ( $<80^{\circ}\text{C}$ ) by technology and material requirements. Recirculation tanks made from recently developed polymeric materials are suitable for use at higher temperatures (53).

Cassetteless transport systems have been developed to reduce the mass of material entering the bath. In these systems wafers are most typically transported between baths by use of a silicon or carbide carrier. These systems have the potential advantage that the amount of contact with the wafer and subsequent transfer of contamination is reduced. The vibrational security of the wafers in the cassetteless system is an area that needs to be addressed.

Immersion processors produce very good results and allow a wide selection of cleaning chemistries, however, chemical usage and floor space requirements are high. In addition, the chemicals in the bath must be monitored and replaced or replenished to ensure consistent results and effectiveness. For further information several references are available (52)-(54)(60)(61).

### **8.3 Spray Processors**

Spray processor systems provide for automatic centrifugal spray cleaning with corrosive or caustic chemicals. They were first introduced by



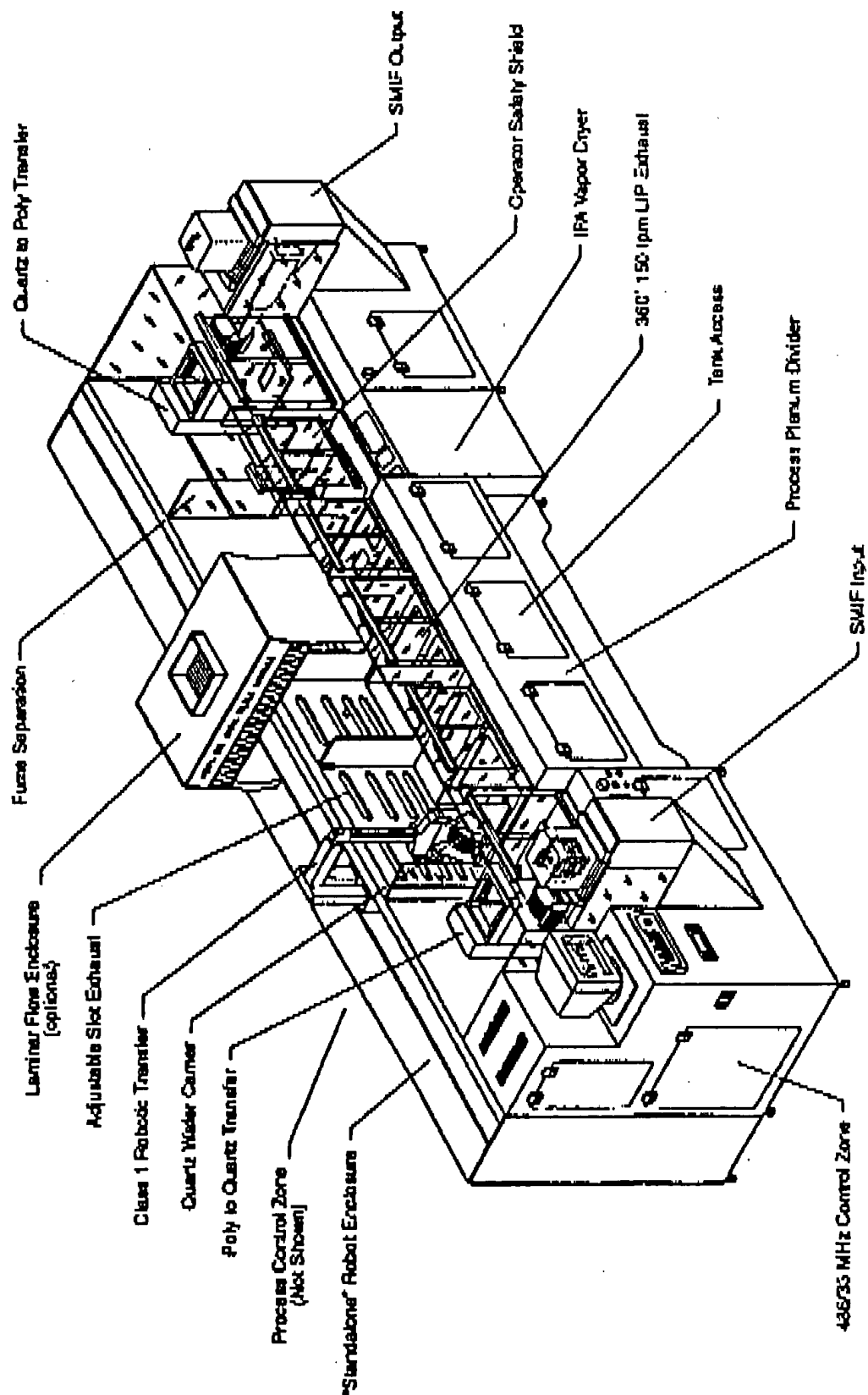


Figure 6. Wet bench for immersion processing [59].

FSI in 1975 (15). In a spray processor, a batch of wafers contained in cassettes is loaded into a turntable that rotates the wafers past a stationary spray post. Filtered acids and reagent solutions are introduced into the chamber through a liquid feed system which includes pressurized spray, a mixing manifold, and nitrogen atomization. The spray is directed uniformly through the spray post at the wafers; the spent chemicals are drained continuously through the bottom of the bowl so that fresh chemicals always contact the wafer. This eliminates solution contamination and degradation problems possible with immersion techniques (52). The system chambers are totally enclosed, with no exposure of the chemicals to the operator or to the environment. Spray processors perform an entire cleaning sequence, including all rinses and a final drying step, without removing the wafers from the equipment. This is achieved by using a microprocessor-based controller that opens and closes pneumatically controlled valves in a programmed sequence. Examples of spray processors are shown in Figs. 7 and 8.

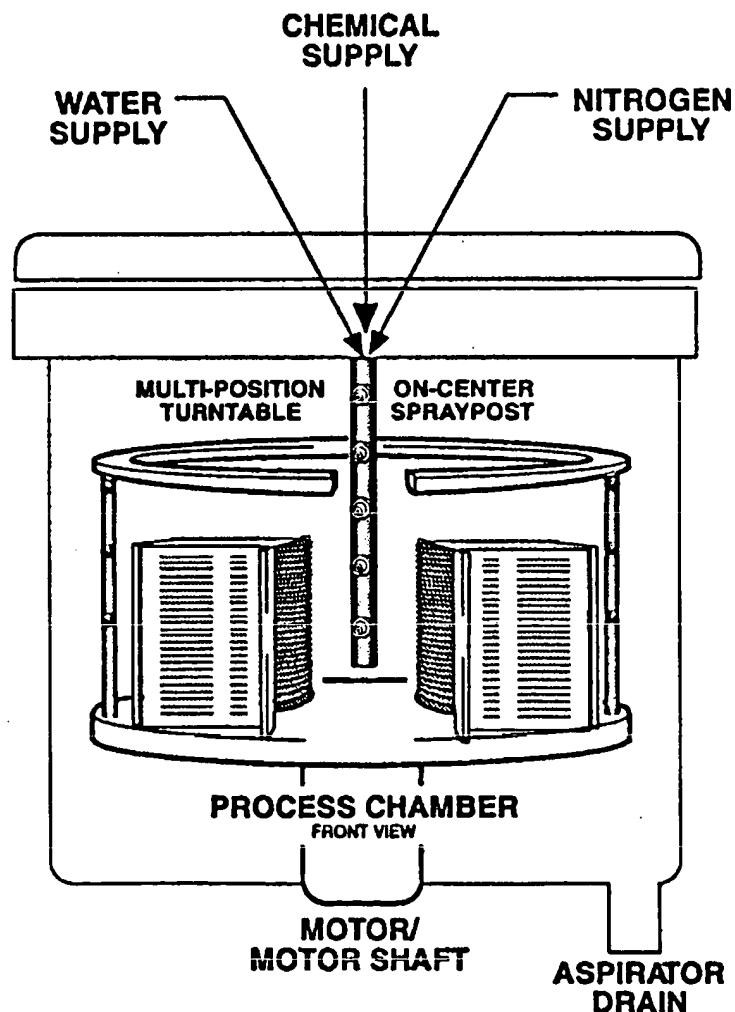
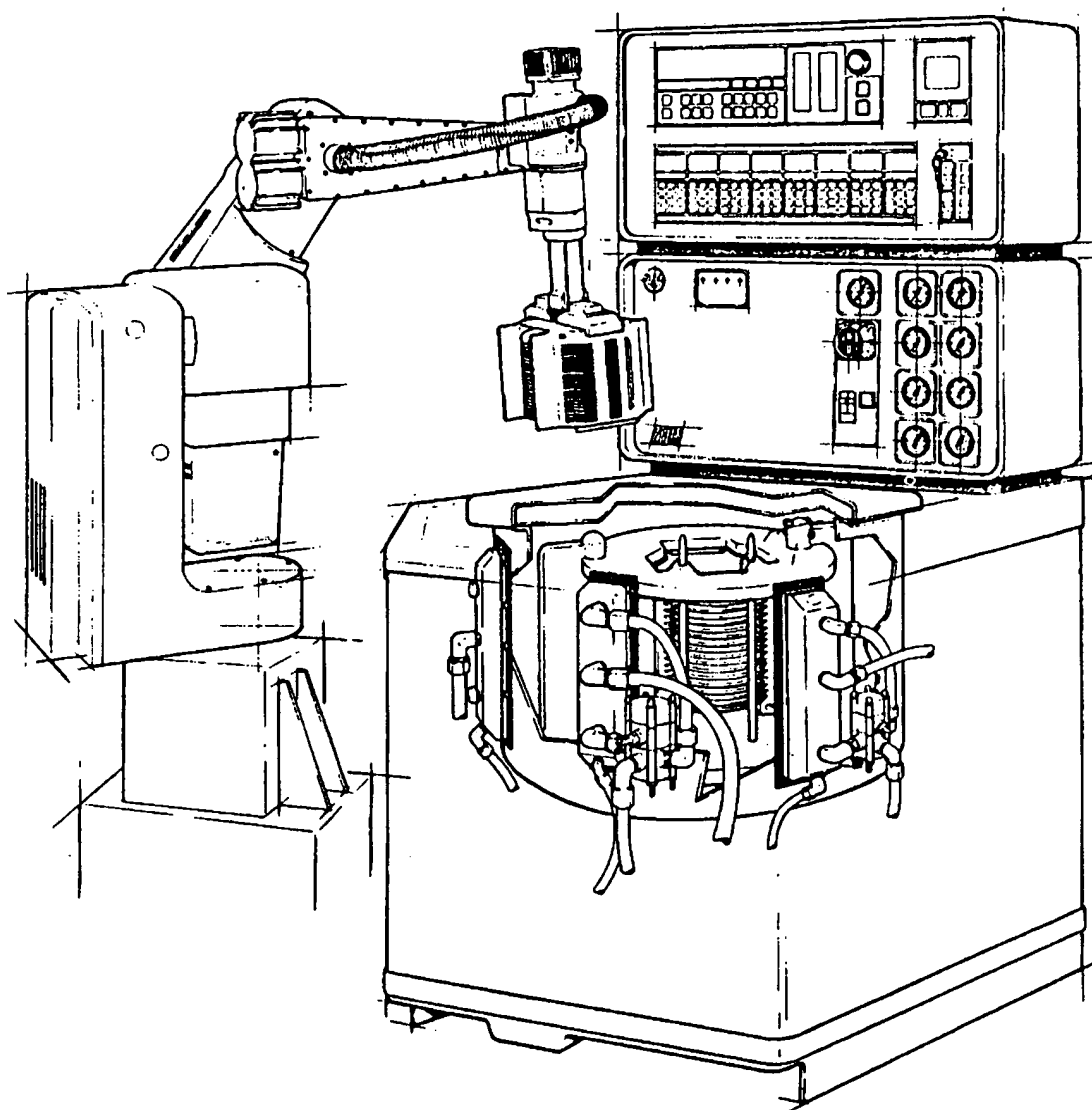


Figure 7. Multiposition spray processor.



**Figure 8.** Spray processor with automatic loading robot.

Spray systems take various forms. High pressure spray helps to physically remove contaminants, but can reduce the time available for surface chemical reactions that are sometimes required for removal of contaminants. Atomization of sprays helps distribute the solution to wafers more efficiently. Although dispensing of fresh chemicals is desirable for minimizing cross-contamination, recirculation of chemicals is acceptable for many processes; such systems are available commercially.

A number of improvements have allowed the original spray system to meet changes in process requirements and more stringent specifications for particle addition and metal contamination, while still providing process flexibility. As in immersion processors, robotics systems have been incorporated. Spray processors have gained acceptance in many places where operator safety, ease of use, floor space, chemical usage, and performance for certain applications are important. Maintenance requirements can be high and provisions must be made for moving parts. For further information several references are available (15)(52)(53).

#### **8.4 Ultrasonics and Megasonics**

Ultrasonic systems have long been used for particle removal and are still used for some applications. Ultrasonic techniques use sonic energy of 10 to 100 kHz passed through a cleaning fluid to dislodge particles on a wafer surface. High intensity sound waves generate pressure fluctuations that result in the formation of cavitation bubbles. Upon collapsing, the bubbles release enough energy to dislodge and disperse particles but can also lead to surface damage (54). It is theorized that cavitation is the cleaning mechanism in ultrasonic cleaning (62).

The use of ultrasonic energy on wafers has always been suspect because of concerns about surface damage due to high temperatures and cavitation bubble explosions. Recent research has been directed toward determining the parameters that can reduce cavitation but still produce effective cleaning (63)(64).

Recent investigations have examined various cleaning fluids for their ability to remove particles from wafers in ultrasonic and spray jet systems. DI water was most effective for removing polymeric particles, while ethanol-acetone (1:1) was most effective, even better than fluorocarbons, for removing inorganic particles. Cleaning efficiency decreases with decreasing particle size (65).

In 1979, researchers at RCA reported on the use of megasonic energy (frequency 700 - 1000 kHz) for removing particles from wafers (32). Because megasonic frequencies are much higher than ultrasonic frequencies, large cavitation bubbles do not have time to form and surface damage should be reduced. In megasonic systems, the energy is produced by an array of piezoelectric crystals or transducers which usually are mounted at the bottom of the tank. The tank contains wafers carried on cassettes immersed in a cleaning liquid, such as SC-1 solution. The impact of

megasonic pressure waves on the wafers enhances the cleaning ability of the cleaning solutions. As stated by Menon et al., "The force required to remove a particle from the wafer surface must be equal to, or exceed, the force of adhesion, and is a function of particle size, particle and wafer surface composition, and the nature of the liquid medium. For a silica particle with a 1 micron diameter (mass =  $5 \times 10^{-13}$  g) that is adhering to a bare silicon surface, the force of adhesion in water is approximately  $4 \times 10^{-4}$  dynes (which is known as the van der Waals force of adhesion). The applied megasonic force acting on this particle can be represented as  $F_{\text{meg}} = \text{mass} \times \text{acceleration}$ . Since the acceleration produced by a megasonic transducer vibrating at a total power of 300 W is approximately  $2.5 \times 10^8$  cm/sec,  $F_{\text{meg}} = 1.25 \times 10^{-4}$  dynes. This megasonic force is approximately of the same magnitude as the force of adhesion; hence, 1 micron particles should be removed from silicon wafers in a megasonic tank containing DI water" (53). Although the higher frequencies inherent to megasonic energy should theoretically be effective for particles smaller than 0.03 microns in diameter, this has not yet been demonstrated.

The enhanced cleaning ability of the SC-1 solution in megasonic systems is due to the combination of its removal capability for organic thin films, its slight Si and SiO<sub>2</sub> etching action, and the force supplied by the megasonic energy for removal of particles. It has been suggested that other chemicals could be used in conjunction with the megasonic energy (28)(29)(52). For example, hydrochloric acid could be used in conjunction with megasonic energy to detach metallic particles, while HF and megasonic energy might work well for removal of silicates.

It should be remembered that a megasonic wafer cleaner can generate particles as well as remove them from wafer surfaces. Deteriorating seals or gaskets and defective transducer-bonding materials can shed particles when the transducers are vibrating. Mechanical movement of the cassette can also be a problem. Improved megasonic systems built under license from RCA have become available in the past few years (52). Equipment makers Vertec, FSI International, and SubMicron Systems have incorporated such innovations as focused spread energy, heated recirculation, liquid coupled transducers, and a variety of tank materials for a wide variety of applications (65)(66).

## 8.5 Liquid Displacement Processors

In 1986, CFM Technologies designed an immersion system which allowed the wafers to remain stationary and enclosed during the entire

cleaning, rinsing and drying process (52). The system was designed to reduce or eliminate potential recontamination resulting from phase boundary crossing, for example, from solution to air. The vessel containing the wafers is hydraulically controlled so that liquids are displaced out of the top as the next process chemical is introduced from the bottom (41). For drying, IPA vapor is introduced through the top to displace the water as it drains out the bottom. Nitrogen drying of the IPA completes the process (67).

## **8.6 Point of Use Chemicals**

Another innovation that has applicability to all types of wet cleaning equipment is the development of point-of-use (POU) chemical generation systems. The aqueous cleaning processes presently used to produce microcircuit devices require chemicals with very low metal ion and particle concentrations. Future devices are expected to require even cleaner chemicals. In the POU process, high-purity filtered gases are bubbled through high-purity water to form solutions such as  $\text{NH}_4\text{OH}$ ,  $\text{HF}$ , or  $\text{HCl}$ . The chemicals formed have very low metal concentrations because both the water and the gases are essentially metal free and metallic extractables from storage containers are minimized. Particle contamination is also low because of the greater filtering efficiency of gases and DI water. Because the technique produces highly pure chemicals it lowers the probability of introducing contamination. In addition, because it can greatly reduce chemical use and cost, the point of use chemical generation technique has high potential for the future.

## **8.7 Single-Wafer Cleaners**

A number of systems have been introduced in the last five years that permit single-wafer cleaning. Some systems are designed as single-wafer spinning systems where the wafer is mounted on a rotating chuck and chemicals are applied through a nozzle over the surface, as in photoresist coating. One system by Dai Nippon Screen has incorporated a megasonic unit in the nozzle. Semitool has also marketed a single-wafer clean system. The driving force for single-wafer systems has been their potential for individual wafer control and improved uniformity especially on large wafers (200 mm or larger). To date, these single-wafer, all-wet systems have not found wide acceptance (3).

### 8.8 Alternative Cleaning Techniques

Many other wet techniques for cleaning silicon wafers have been tried over the years with varying degrees of success. Some techniques are limited to specific applications by their undesirable side effects. An example is wet-chemical etching of silicon to remove entire surface layers by etch dissolution. The following techniques have been found viable and, in some cases, can be a desirable addition or alternative to the conventional processes based on hydrogen peroxide solutions.

**Brush Scrubbing.** Removal of large particles, such as those left after sawing and lapping operations, has been accomplished since the early days with wafer scrubbing machines. Brushes made of a hydrophilic material, such as nylon, dislodge particles hydrodynamically while DI water or isopropyl alcohol is applied to the surface. A thin layer of fluid must be retained between the brush and the wafers by careful mechanical adjustment to prevent surface scratching. While many contradictory claims have been made, if properly maintained, brush scrubbing can be very effective for removing particles larger than 1 micron from planar and preferably hydrophilic wafer surfaces (52)(68).

**Fluid Jet.** High pressure fluid jet cleaning consists of a high velocity jet of liquid sweeping over the surface at pressures of up to 4000 psi. The liquid can be DI water or organic solvents. The shear forces effectively dislodge submerged particles and penetrate into topography, but damage to the wafer can result with improperly adjusted pressure (52)(68).

### 8.9 Combined Wet/Dry Systems

As effective "dry cleaning" process steps are developed, systems which combine wet and dry processing may find niches in the market. An example of this type of system is the Excalibur In Situ Rinse\*. In this equipment anhydrous HF and water vapor are used to etch the oxide on a wafer surface. The metals and other contaminants that are embedded in the oxide and at the oxide-silicon interface are removed in a subsequent water rinse. Wafers cleaned in this manner have extremely low residual metal contamination levels (69). Both the etching step and the rinse are performed in a single chamber resulting in a compact system.

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\*Excalibur In Situ Rinse is a registered trademark of FSI International, Chaska, Minnesota.

## 8.10 Rinsing and Drying

Because rinse tanks and dryers can be major sources of particulate contamination, systems and the process procedures used must be investigated thoroughly. The proper design of the rinse and dry steps is especially critical in HF-last type cleaners where hydrophobic surfaces are produced. The quick-dump rinse tanks with top spray rapidly remove chemicals from the wafer surfaces and periodically drain the chemical solution (54). However, problems with bacterial growth in parts of the system, especially the nozzle, and the inherent turbulence which can move particles through the solution make this method of rinsing less desirable from a particle contamination standpoint.

Another common rinse system, the cascade overflow system, is less susceptible to particle contamination. Hot water is often used for cascade rinses when viscous chemicals such as sulfuric and phosphoric acids need to be removed. The hot water adds cost to the system, but potentially reduces the number of particles on the finished dry wafer.

The final rinse technique is most often combined with a spin dryer to form the ubiquitous spin rinse/dryer, shown in Fig. 9. Water is sprayed on the wafers as they rotate in a chamber, as in spray processors. After the rinse, the wafers are spun dry, often with nitrogen flowing through the chamber. The chamber needs to be designed such that water on the walls after the rinse is not deposited on the wafer. Many users, to avoid this possibility, use the rinse dryer to dry wafers that have been rinsed in another system, such as a cascade overflow tank. Recently, dryers have been introduced which eliminate the rinse function. The wafers are spun dry in a chamber that allows massive quantities of HEPA filtered air to flow in the top and out through the exhaust. These have been termed *downflow* devices and have met with some success (55).

Several other techniques for drying have been proposed and investigated, such as hot nitrogen drying, vacuum drying, and slow pull drying (Sec. 7.3), but the technique that has garnered the most interest is IPA vapor drying (Sec. 7.2). Vapor drying systems should potentially leave fewer particles than spin-dry systems, but superiority has yet to be demonstrated. In addition, there is some concern over organic residues being left behind. The technique has been slowly gaining acceptance, especially due to its lack of mechanical motion and small number of moving parts in the system.



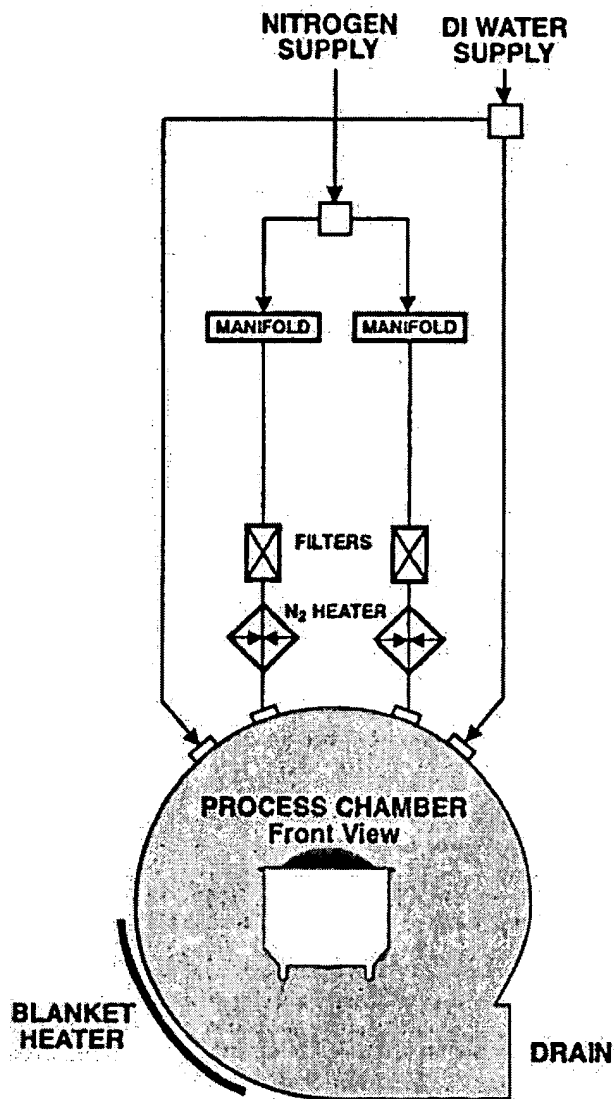


Figure 9. Schematic diagram of a spin rinser/dryer.

## 9.0 CONCLUSION

Although it may initially appear that aqueous cleaning of semiconductor wafers is a technology that is in the decline phase of its life cycle, it should now be clear that it, like many other technologies, is extending its time horizon of utility for a number of reasons that have been discussed in this chapter. The chief driving forces for the preservation of aqueous cleaning technology include the superior ability to remove metallic impurities, the high level of selectivity between the contaminants and the semiconductor surface, and the improvements in efficiency in use of aqueous cleaning agents to lower the cost and lessen the environmental effects.

It is clear that there is continuing R & D effort being expended for refining aqueous cleaning chemistries and equipment to achieve the needed improvements. Some of these efforts are directed toward greater contaminant removal to keep up with the ever increasing requirements of the semiconductor device manufacturers for cleaner wafers. Likewise, there is a real need to tailor the cleaning process (chemistry, sequence, and apparatus) to the needs of specific applications. This is sometimes referred to as *application specific cleaning*, which is the logical step to take since there is no universal best cleaning process. There are, and will continue to be, trade-offs in choosing the best procedure for a given situation. This logic can be extended to suggest that a combination of dry cleaning and wet (aqueous) cleaning of semiconductor wafers will be used for the foreseeable future.

## REFERENCES

1. Feder, D. O. and Koontz, D. E., *Symposium on Cleaning of Electronic Device Components*, ASTM STP No. 246, pp. 40-63 (1959)
2. Mittal, K. L., in: *Surface Contamination: Genesis, Detection, and Control*, (K. L. Mittal, ed.), 1:3-45, Plenum Press, New York (1979)
3. Confidential communication with members of a semiconductor firm.
4. Hirschfelder, J. O., Curtiss, C. F. and Bird, R. B., *Molecular Theory of Gases and Liquids*, John Wiley and Sons, New York (1954)
5. Good, R. J., in: *Treatise on Adhesion and Adhesives*, Vol. 1, Chap. 2, (R. L. Patrick, ed.), Marcel Dekker, New York (1967)
6. Whitfield, W. J., in: *Surface Contamination: Genesis, Detection and Control*, (K.L. Mittal, ed.), 1:73-81, Plenum Press, New York (1979)
7. Pudvin, J. F., in: *Environmental Control in Electronic Manufacturing*, (P. W. Morrison, ed.), pp. 146-178, Van Nostrand Reinhold Company, New York (1973)
8. Kern, W., *RCA Review*, 31:207-233, (1970)
9. Hildebrand, J. H., in: *The Encyclopedia of Chemistry* (C. A. Hampel and G. G. Hawley, eds.), 3:1018-1021, Van Nostrand Reinhold Company, New York (1973)
10. Mittal, K. L., in: *Surface Contamination: Genesis, Detection, and Control*, (K. L. Mittal, ed.), 1:9-10, Plenum Press, New York (1979), and references therein.

11. Lange, N. A., in: *Lange's Handbook of Chemistry*, Revised 10th Edition, McGraw-Hill, Inc. (1967)
12. Amick, J. A., *Solid State Technology*, 19(11):47-52 (1976)
13. Kern, W. and Puotinen, D., *RCA Review*, 31:87-206 (1970)
14. Kern, W., *Proc. First International Symposium on Cleaning Technology in Semiconductor Device Manufacturing/1989*, 90-9:3-19, (J. Ruzyllo and R. E. Novak, eds.), The Electro-chemical Society, Pennington, NJ (1990)
15. Burkman, D. C., *Semiconductor International*, 4(7):103-114 (1981)
16. Muroakor, H., Kurosawa, K., Hiratsuka, H. and Usami, T., *Electrochem. Soc. Ext. Abstracts*, No. 238, 81-2:570 (1981)
17. van Zant, P., *Semiconductor International*, 7(4):109-111 (1984)
18. Davidson, J. and Hoffman J., *Proc. First International Symposium on Ultra Large Scale Integration Science and Technology*, pp. 798-804, (S. Broydo and C. M. Osburn, eds.), The Electrochemical Society, Pennington, NJ (1987)
19. Tong, J. T., Grant, D. C., and Peterson, C. A., *Proc. Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, 99-12:18-25, (J. Ruzyllo and R. E. Novak, eds.), The Electrochemical Society, Pennington, NJ (1992)
20. Takizawa, R. and Ohsawa, A., *Electrochem. Soc. Ext. Abstracts*, No. 387, 89-2:564 (1989)
21. Imaoka, T., Kezuka, T., Takano, J., Sugiyama, I. and Ohmi, T., *Proc. 38th Annual Technical Meeting Institute of Environmental Sciences*, pp. 466-474, The Institute of Environmental Sciences, Mount Prospect, IL (1992)
22. Kikuyama, H. and Miki, N., *Proc. 9th International Symposium on Contamination Control*, pp. 387-383, The Institute of Environmental Sciences, Mount Prospect, IL (1988)
23. Henderson, R. C., *J. Electrochem. Soc.*, 119(6):771-775 (1972)
24. Kern, F., Jr., Mitsushi, I., Kawanabe, I., Miyashita, M., Rosenberg, R. W. and Ohmi, T., "Metallic Contamination of Semiconductor Devices From Processing Chemicals, The Unrecognized Potential," Presented at 37th Annual Technical Meeting in San Diego, CA, Institute of Environmental Sciences (1991)
25. Riley, D. J. and Carbonnel, R. G., *Proc. 37th Annual Technical Meeting*, pp. 886-891, The Institute of Environmental Sciences, Mount Prospect, IL (1991)

26. Milner, T. A. and Brown, T. M., *Proc. Microcontamination Conf. and Exposition*, pp. 146-156 (1986)
27. Menon, V. B. and Donovan, R. P., *Proc. First International Symposium on Cleaning Technology in Semiconductor Device Manufacturing/1989*, 90-9:167-181, (J. Ruzyllo and R. E. Novak, eds.), The Electrochemical Society, Pennington, NJ (1990)
28. Atsumi, A., Ohtsuka, S., Munehira, S. and Kajiyama, K., *Proc. First International Symposium on Cleaning Technology in Semiconductor Device Manufacturing/1989*, 90-9:59-66, (J. Ruzyllo and R. E. Novak, eds.), The Electrochemical Society, Pennington, NJ (1990)
29. Menon, V. B., Clayton, A. C. and Donovan, R. P., *Microcontamination*, 7(31):31-34, 107-109 (1989)
30. Peterson, C. A., Schmidt, W. R., Burkman, D. C. and Phillips, B. F., *Proc. Technical Programme Semiconductor 1983 International*, presented in Birmingham, England (27-29 September, 1983). Also available as FSI Technical Report 217 from the authors.
31. Watanabe, M., Harazono, M., Hiratsuka, Y. and Edamura, T., *Electrochem. Soc. Ext. Abstracts*, 81-3:221-222 (1983)
32. Shwartzman, S., Mayer, A. and Kern, W., *RCA Review*, 46:81-105 (1985)
33. Slusser, G. J. and MacDowell, L., *J. Vac. Sci. Technology*, A-5(4):1649-1651 (1987)
34. Kawado, S., Tanigaki, T. and Maruyama, T., *Semiconductor Silicon 1986, Proc. Fifth International Symposium on Silicon Material Scientific Technology*, pp. 989-998, (H. R. Huff, T. Abe, and B. Kolbesen, eds.), The Electrochemical Society, Pennington, NJ (1986)
35. Seitaro, S. I. and Tanaka, F., *Proc. 9th International Symposium on Contamination Control*, pp. 374-377, The Institute of Environmental Sciences, Mount Prospect, IL (1988)
36. Lampert, I., *Electrochem. Soc. Ext. Abstracts*, 87-1:381-382 (1987)
37. Gould, G. and Irene, E. A., *J. Electrochem. Soc.*, 174(4):1031-1033 (1987)
38. Ruzyllo, J., *Technical Proc. Semicon/Europa, 1986*, pp. 1869-1870, Zurich (March 3-6, 1986)
39. Becker, D. S., Schmidt, W. R., Peterson, C. A. and Burkman, D., in: *Microelectronics Processing, Inorganic Materials Characterization*, Chap. 23, ACS Symp. Series No. 295, pp. 368-376, (L. A. Casper, ed.), American Chemical Society, Washington, DC (1986)

40. Christenson, K., *Proc. Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, 92-12:286-293, (J. Ruzyllo and R. E. Novak, eds.), The Electrochemical Society, Pennington, NJ (1992)
41. Walter, A. E. and McConnell, C. F., *Microcontamination*, 8(1):35- 61 (1990)
42. Krusell, W. C. and Golland, D. I., *Proc. First International Symposium on Cleaning Technology in Semiconductor Device Manufacturing/ 1989*, 90-9:23-32, (J. Ruzyllo and R. E. Novak, eds.), The Electrochemical Society, Pennington, NJ (1990)
43. Takizawa, R. and Ohsawa, A., *Proc. First International Symposium on Cleaning Technology in Semiconductor Device Manufacturing/1989*, 90-9:75-82, (J. Ruzyllo and R. E. Novak, eds.), The Electrochemical Society, Pennington, NJ (1990)
44. Kern, W., *Semiconductor International*, 7(4):94-99 (1984)
45. Ohmi, T., Mishima, H., Mizuniwa, T. and Abe, M., *Microcontamination*, 7(5):25-32, 108 (1988)
46. Grundner, M., Hahn, P. I., Lampert, I., Schnegg, A. and Jacob, H., *Proc. First International Symposium on Cleaning Technology in Semiconductor Device Manufacturing/1989*, 90-9:215-226, (J. Ruzyllo and R. E. Novak, eds.), The Electrochemical Society, Pennington, NJ (1990)
47. Shaw, D. J., *Introduction to Colloid and Surface Chemistry*, 2nd Edition, p. 118, Butterworth, London (1979)
48. Blum, R., Personal communication with D. Grant (1991)
49. Goodman, J. and Mudrak, L., *Solid State Technology*, 31(10):37-39 (1988)
50. Goodman, J. and Andrews, S., *Solid State Technology*, 33(7):65-68 (1990)
51. Skidmore, K., *Semiconductor International*, 12(8):80-86 (1989)
52. Kern, W., *J. Electrochem. Soc.*, 137(6):1887-1892 (1990) (This paper was originally presented at the 1989 Fall Meeting of The Electrochemical Society, Inc. held in Hollywood, FL.)
53. Menon, V. B. and Donovan, R. P., *Microcontamination*, 8(11):29-34, 66 (1990)
54. Skidmore, K. *Semiconductor International*, 9(9):80-85 (1987)
55. Mishima, H., Yasui, T., Mizuniwa, T., Abe, M. and Ohmi, T., *IEEE Transactions on Semiconductor Manufacturing*, 2(3):69-75 (1989)

56. Figure provided by Robert Orr, Trebor Incorporated, West Jordan, Utah.
57. du Pont Bulletin, No. E-08572, E. I. du Pont de Nemours & Company, Wilmington, Delaware
58. du Pont Bulletin, No. E-21623-1, E. I. du Pont de Nemours & Company, Wilmington, Delaware
59. Figure provided by R. Novak, SubMicron Systems, Inc., Wayzata, MN.
60. "Wafer Cleaning Equipment, 1986 Master Buying Guide," *Semiconductor International*, 8(13), pp. 76-77 (1986)
61. Singer, P. H., *Semiconductor International*, 11(8):42-48 (1988)
62. Suslick, K., *Sci. American*, 260(2):80-86 (1989)
63. Kashkoush, I., Busnaina, A., Kern, F. and Kunesch, R., *Proc. 36th Annual Technical Meeting*, pp. 407- 413, Institute of Environmental Sciences, Mount Prospect, IL (1990)
64. O'Donoghue, M., *Microcontamination*, 2(5):63-67 (1984)
65. Menon, V. B., Michaels, L. D., Clayton, A. C. and Donovan, R. P., *Proc. 35th Annual Technical Meeting*, pp. 320-324, Institute of Environmental Sciences, Mount Prospect, IL (1989)
66. Mayer, A. and Shwartzman, S., *J. Electronic Materials*, 8(6):855-863 (1979)
67. McConnell, C. F., *Proc. 36th Annual Technical Meeting*, pp. 269-272, Institute of Environmental Sciences, Mount Prospect, IL (1990)
68. Burggraaf, P. S., 4(8):71-102 (1981)
69. Syverson, D., *Proc. 37th Annual Technical Meeting*, pp. 829-833, Institute of Environmental Sciences, Mount Prospect, IL (1991)

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## Vapor Phase Wafer Cleaning Technology

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*Bruce E. Deal and C. Robert Helms*

### 1.0 INTRODUCTION AND BACKGROUND

#### 1.1 General

Cleaning of silicon wafers has been an integral part of semiconductor device fabrication since the 1950s, when silicon replaced germanium as the preferential semiconductor material. Now, as in the past, types of impurities encountered include oxides, heavy metals, alkali and other light elements, organics, and particles and residues of all kinds. In the proceedings of the first major symposium devoted to cleaning of electronic device components and materials in 1958 (1), two conclusions are apparent. First, similar procedures were used for cleaning silicon and germanium wafers and for tube materials. Second, until recently, the same types of aqueous batch cleaning processes have been used continuously during device fabrication (2), even though device complexity has increased from single transistors on 15 mm diameter wafers to complex integrated circuits containing more than one million components on 200 mm diameter wafers. Furthermore, as feature size decreased from mils to angstroms, and process complexity increased from the use of a few masking steps to twenty or more, and as process steps now number in the several hundred compared to a little more than a dozen in 1960, many of the process procedures used to fabricate devices have remained relatively unchanged in principal. The same is also true for the materials used in the device structures.

The above-mentioned conservative nature of semiconductor process and device engineers has continued to be apparent in the cleaning area as was demonstrated by a survey report a few years ago. In this report, it was concluded that "only one-third of the industry is working on new cleaning or monitoring methods." The "remainder are content in their ways" (3). This finding was even more surprising when it is considered that at that time, newer methods of masking lithography, etching, metal deposition, oxidation, and other processes were being actively pursued and implemented.

Fortunately, more recently, newer methods of wafer cleaning have been developed and are starting to be implemented. One of these, vapor phase cleaning, is the subject of this chapter. After a brief review of trends in wafer cleaning since 1960 and the conclusion that many of the so-called "improved" methods also have had shortcomings, vapor phase cleaning technology is discussed. First, historical developments of vapor cleaning are summarized, with discussions of the various types of systems and processes used. Next, the subject of vapor phase etching of oxides and dielectrics is reviewed, including a discussion of mechanisms involved. A critical aspect of wafer cleaning is the removal of trace impurities from the wafer surface and both analysis techniques (briefly summarized) as well as removal procedures using vapor phase technology are discussed. Perhaps the most important, and certainly the subject of greatest interest to the device engineer, is the effectiveness of the cleaning procedures with respect to device applications. Such results are presented in some detail for particular areas. Finally, recent developments involving advanced processing of semiconductor device wafers are reviewed. It is observed that cleaning and related technologies may actually "drive" the overall direction of device manufacturing. This is already resulting in the development and evaluation of various types of in situ, sequential processing involving cluster tool systems, also referred to as integrated processing. This concept is discussed in detail. The chapter ends with a summary of possible future trends in vapor cleaning of silicon wafers, including device requirements, possible new vapor chemistries, and other related topics.

It should be noted that most of the cleaning technology discussed in this chapter deals with silicon wafers. This is because a large percentage of today's semiconductor devices are silicon, and extensive cleaning efforts on other materials cannot be justified at present. On the other hand, cleaning problems associated with compound semiconductors are even more complex than silicon and will require even more effort to solve them. Undoubtedly, many of the advantages of vapor cleaning discussed in this



chapter can also apply to such materials as gallium arsenide. Consequently, as this newer technology matures, it will very likely be used to advance the state-of-the-art processing for compound semiconductors.

## **1.2 Aqueous Cleaning Processes**

It was mentioned above that the original wafer cleaning methods employed in the late 1950s and early 1960s were a carry-over from tube material cleaning procedures. In the late 1960s, the invention of integrated circuits and MOS device structures required improved procedures for cleaning wafers. These have been reported by Kern and Puotinen (4)-(7) and others (8)-(11), but still resemble the same type of aqueous processes used earlier. Typical sequences included solutions of acids ( $\text{H}_2\text{SO}_4$ ,  $\text{HCl}$ ) or bases ( $\text{NH}_4\text{OH}$ ) with hydrogen peroxide, followed by appropriate deionized water rinses. In addition, an aqueous HF treatment was frequently used in various parts of the sequence. Kern has recently reviewed these developments (6) and they are also discussed in Ch. 3 of this volume. Some of the shortcomings of aqueous cleaning technology include:

1. Ineffective in cleaning small geometries
2. Contributes additional contamination and particles
3. High cost of chemicals
4. Environmental problems

Attempts have been made to overcome some of these problems. Approaches have included spray cleaning (12), displacement processing (13), jet aerosol cleaning (14), megasonics (15), recirculation of chemicals (16), and others (17). Along with the cleaning solutions themselves, severe problems have also been attributed to the deionized water rinse and drying steps. More often than not, the wafers were cleaner before these steps than after. Even with considerable efforts to provide satisfactory aqueous cleaning procedures, it was not believed that such cleaning technology would keep up with the requirements of the rapidly advancing device complexity.

## **1.3 "Dry" Cleaning Processes**

Another approach to wafer cleaning involved the so-called "dry" processing. As early as 1960, when epitaxial technology was developed, it was found that a gas-phase in situ hydrochloric acid predeposition etch

improved the epi-film quality (18)-(21). Soon, process engineers were experimenting with various gases, such as chlorine (22), hydrogen fluoride-hydrogen iodide (23), and other halides (24)(25). Because of the high temperatures required, it wasn't long before some sort of excitation was employed, such as reactive ions, ultraviolet light, plasmas, electron cyclotron resonance, and RF sputter or microwave radiation, in order to lower the process temperature. While these processes have demonstrated some value in wafer cleaning, it is now apparent that various problems are associated with them (26)-(28). The main difficulty has to do with the adverse radiation effects on the device structures themselves (29)-(31). In addition, various contamination problems are observed, both from bombardment of materials in the systems, and due to the formation of undesirable reaction byproducts from the complex chemistries involved. Some of these byproducts, such as polymers, are extremely difficult to remove from the wafer surfaces.

#### **1.4 Other Types of Cleaning Processes**

One other type of non-aqueous cleaning procedure that has been reported by several investigators is so-called ice, jet, or snow scrubbing (32)(33). In this method, jets of solid  $\text{H}_2\text{O}$  or  $\text{CO}_2$  ice particles are directed at the wafer surface at high velocity. Some success has been reported in removing various organic films, but problems of non-uniformity and surface damage have prevented this procedure from moving from the laboratory to production.

An important type of dry cleaning procedure used to clean silicon wafers has involved ultraviolet light with ozone ( $\text{UV/O}_3$ ) (34)(35). As in the case with aqueous cleaning procedures, various "dry" cleaning techniques including  $\text{UV/O}_3$  and other related technologies are discussed more completely in Chs. 5 and 6 of this volume.

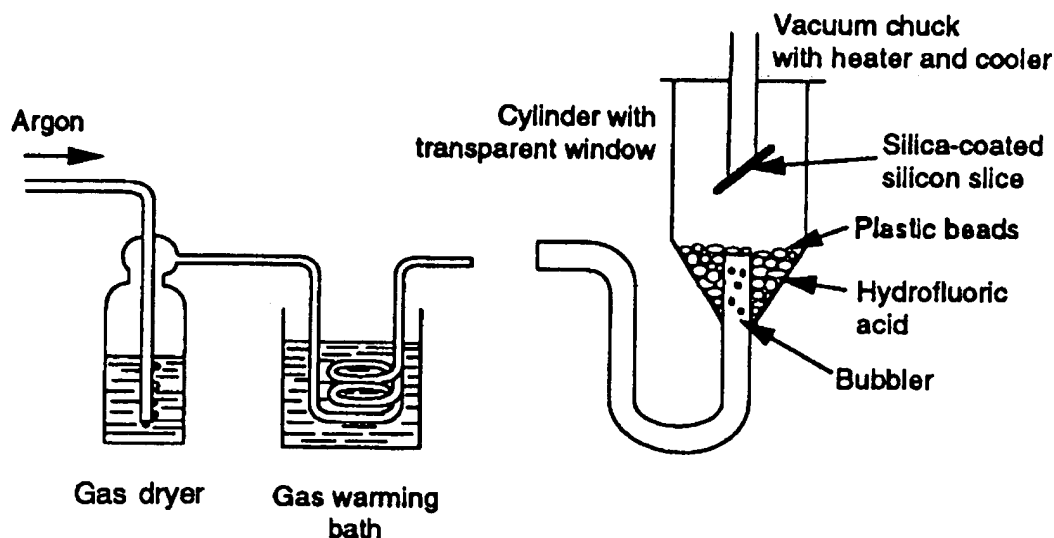
## **2.0 VAPOR CLEANING**

### **2.1 Historical**

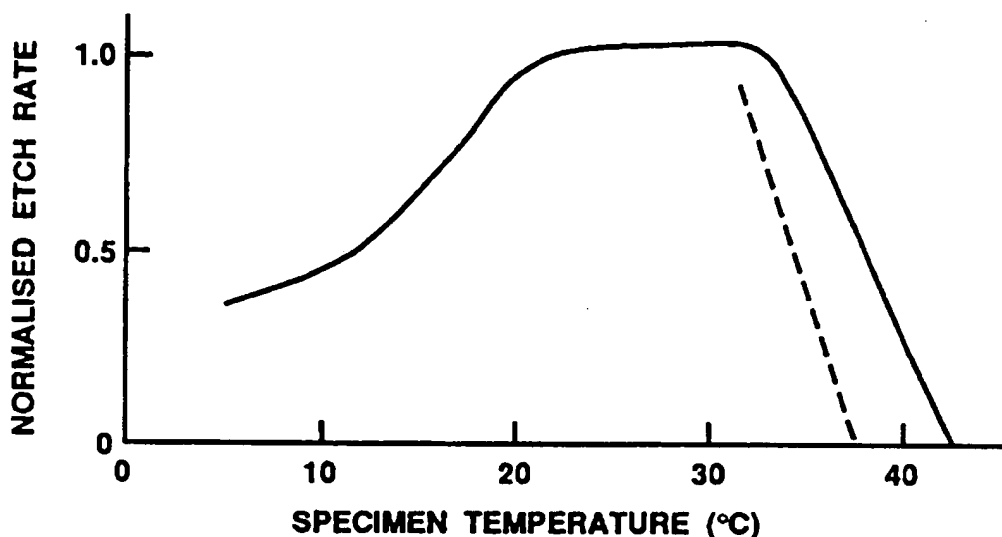
The concept of vapor phase or gas processes for removing oxides has been known for a number of years. The original paper describing vapor HF removal of silicon oxide was written by Holmes and Snell in 1966 (36). A schematic diagram of the apparatus used is shown in Fig. 1. In their

experiments, the authors suspended an oxidized silicon wafer above an aqueous solution of hydrofluoric acid. The solution was agitated by dry argon which also helped to transport the  $\text{HF}/\text{H}_2\text{O}$  to the wafer. Oxide etch rates were determined as a function of HF concentration and temperature. The authors observed that "the rate of attack of the oxide by the vapor close above the etching bath was comparable with that in the bath." Two other key results from this early work were that the reaction rate followed the familiar "volcano plot" peaking in their experiments at  $20^\circ$  to  $30^\circ\text{C}$  and falling to zero rapidly at higher ( $\sim 40^\circ\text{C}$ ) temperatures. This plot is reproduced in Fig. 2. They also suggested the importance of surface condensation which, as will be shown below, is a key factor in oxide etching. These and other results of Holmes and Snell provide insight into etch mechanisms only now being completely understood (37)-(39). Those authors made use of information concerning vapor pressures of HF and  $\text{H}_2\text{O}$  in aqueous HF solutions at various temperatures reported in the 1940s by Brosheer and co-workers (40), by Munter and co-workers (41)(42), and by others (43)-(45). These data are still valid today.

Subsequent to the work of Holmes and Snell, Beyer and Kastl (46) also investigated a process based on vapor phase  $\text{HF}/\text{H}_2\text{O}$  mixtures for etching  $\text{SiO}_2$  as did Blackwood, Biggerstaff, Clements, and Cleavelin (47). These investigators also observed the results to be similar to those obtained in  $\text{HF}/\text{H}_2\text{O}$  liquid phase processing.



**Figure 1.** Equipment for experiments on etching of silica with a controlled flow of hydrofluoric acid vapor; after Holmes and Snell (36).



**Figure 2.** Etch rate of silica by hydrofluoric acid vapor at 24°C as a function of specimen temperature; after Holmes and Snell (36). Full line - 40% acid; broken line - dilute acid.

As noted later in this chapter, the mechanism for HF etching of  $\text{SiO}_2$  involves an initial requirement for water availability before etching begins, even though water is a product of the reaction. An interesting application related to this effect was reported in 1977 by Bersin and Reichelderfer (48). In this case, the oxide etching was carried out selectively under a negative photoresist layer which contained enough water to initiate the reaction. In areas with no resist, the oxide etching did not occur.

About the same time as Holmes' work with vapor HF etching of silicon oxide, the use of HCl was reported as a pre-epitaxial silicon clean of the silicon substrate (18)(19). It was shown that by exposing the silicon substrate to HCl vapor at 1150° to 1250°C immediately prior to epitaxial deposition (in situ), low defect epi material could be deposited. The trend today towards low temperature (<1000°C) silicon epi deposition has caused process engineers to develop other in situ cleans such as vapor HF, but HCl is still used commercially in most production applications.

As mentioned earlier, a number of other gases have been evaluated during the past twenty-five years for cleaning or etching silicon as well as silicon dioxide surfaces. These have included halogen fluorides, such as  $\text{ClF}_3$ ,  $\text{BrF}_3$ , and  $\text{IF}_3$  (49), and other fluorides including  $\text{NF}_3$ ,  $\text{BF}_3$ ,  $\text{PF}_3$ , and  $\text{PF}_5$  (50). Some of these procedures involved excitation of some kind, such as plasma; others did not. As of this date, few, if any, have been used for high volume device manufacturing applications.

In the employment of aqueous cleaning processes, various types of drying techniques have been used (51)-(54). These normally follow some sort of deionized water rinse, either a dip or spray. The drying steps consisted of blowing nitrogen, spinning, heating (in a hot inert ambient, vacuum, or infrared radiation), or immersing in a volatile organic liquid or vapor, such as isopropanol (53). Most of these drying techniques would be considered *vapor* or *dry* in nature. Certainly they could be compatible with vapor type cleaning processes. The subject of drying silicon surfaces in general is not completely understood or modeled from a mechanism standpoint, and is discussed more completely in a later section.

### 2.2 Advantages of Vapor Cleaning

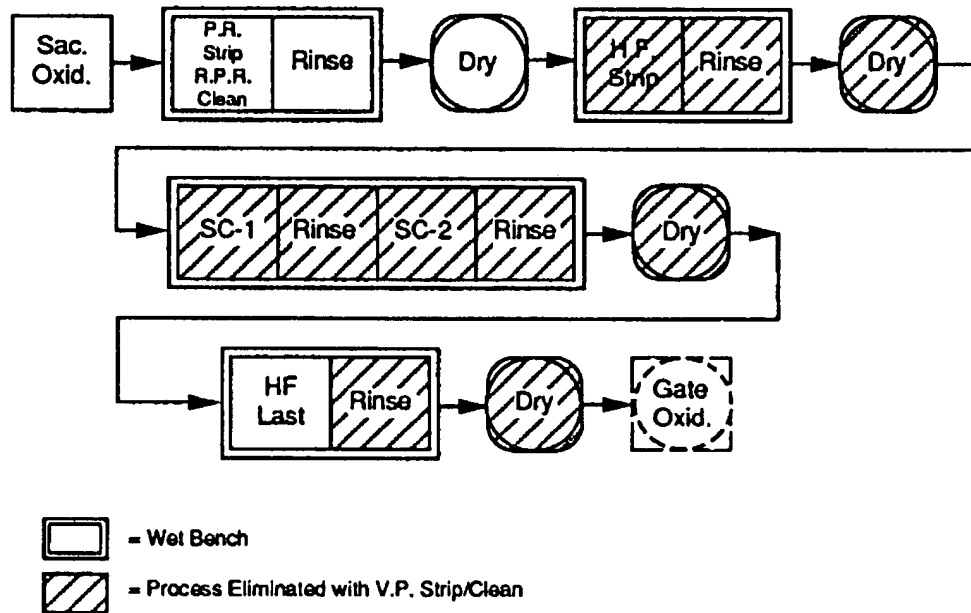
During the development of improved wafer cleaning processes over a number of years, distinct advantages of vapor or gas phase cleaning have been demonstrated. Some of these are indicated here.

**Reduced Contamination.** One of the problems associated with conventional aqueous cleaning processes has been the redepositing of contaminants of various types back on the wafers. This has been observed in both the cleaning solution itself, as well as in the deionized water rinsing and drying steps. In the case of vapor processes, this self-contamination has not been observed, and very good results are typically obtained.

**Improved Process Uniformity.** Typically, as smaller and controlled amounts of reactants are used in a semiconductor fabrication process, better control is achieved for both the specific reaction involved and the overall process. This improvement has been noted in various process steps, and a good example is ion implantation versus furnace pre-deposition. Similarly, gas phase reactions of vapor etching have also resulted in superior control of etch selectivity, uniformity, and repeatability.

**Reduced Chemical Usage and Disposal.** An important consideration in today's manufacturing processes is that of environmental effects. Even though electronics manufacturing has been referred to as the "clean" industry, nevertheless, severe contamination problems have occurred in certain areas such as "Silicon Valley," California. Mainly affected have been ground water supplies through faulty storage tanks. Since gas or vapor phase cleaning typically uses less than 1/100 of a given chemical than does aqueous cleaning, considerable reduction of environmental problems as mentioned above will occur. Thus, the cost of the manufacturing is reduced as well as environmental contamination effects. An example of how vapor phase cleaning could replace several liquid cleaning, rinsing,

and drying steps in a typical wafer processing sequence (MOS gate oxidation) is shown in Fig. 3.



**Figure 3.** Potential replacement of individual processes in conventional aqueous cleaning sequence by vapor phase cleaning technology. (Courtesy of Advantage Production Technology).

**Improved Safety Considerations.** Along the lines of environmental improvements discussed above, vapor phase processing also provides a much safer working condition than encountered in typical *wet-bench* cleaning facilities. In addition, device processing may be carried out much more efficiently. Vapor cleaning is more adaptable to computer controlled processing and results are significantly improved because of this.

**More Versatile Process Variables.** Gas or vapor type processing allows much more versatility in the range of process variables permitted than do liquid or aqueous systems. For instance, it is much easier to vary either temperature or pressure in vapor systems. Thus, relative compositions of gas mixtures can be varied over a wide range, and resulting chemistries can be adjusted for particular applications. Furthermore, the volatility of certain reaction products can be maximized. Also, at reduced pressures it is possible for the reactants to penetrate narrow openings and to effect removal of unwanted materials from these openings.

**New Chemistries Possible.** Just about any liquid chemistry can be converted to gas or vapor phase. In addition, many additional gas species are available for improved chemical cleaning applications. It is anticipated that such new chemistries will be employed for the more efficient removal of all types of contaminants.

**Sequential, In Situ Processing Possible.** Perhaps one of the greatest advantages of vapor phase wafer cleaning will be its suitability for so-called integrated or cluster-type processing. Such capability will permit various pre-process cleaning steps for the more critical applications. This subject is discussed more completely in Sec. 7.

### 2.3 Current Vapor Cleaning Systems

At the present time, at least two systems employing vapor phase chemistries are being used for cleaning silicon wafers. These are briefly described below in chronological order.

**Anhydrous Hydrogen-Fluoride/Water-Vapor.** The industry's first commercial vapor phase etching tool was FSI International's Excalibur\* system (55)-(57). Designed jointly with Texas Instruments for the etching of  $\text{SiO}_2$ , the system was introduced commercially in 1987. Operating at ambient temperature and pressure, the single wafer system provides a controlled mixture of anhydrous HF and  $\text{H}_2\text{O}$  vapor to the process chamber using programmable mass flow controllers. The  $\text{N}_2$  carrier gas, anhydrous HF and the  $\text{H}_2\text{O}$  vapor ratios can be varied to satisfy selectivity requirements for etching dissimilar oxides simultaneously. Figure 4 provides a schematic diagram of the key components.

The initial systems used in production were etch-only systems that proved effective for thin etches, especially native oxide removal before CVD processes. An integrated rinse feature, added later, provided improved performance by reducing particles on the wafer and removing metallic and dopant residues resulting from various etches required for pre-CVD pre-gate and pre-contact processes (58).

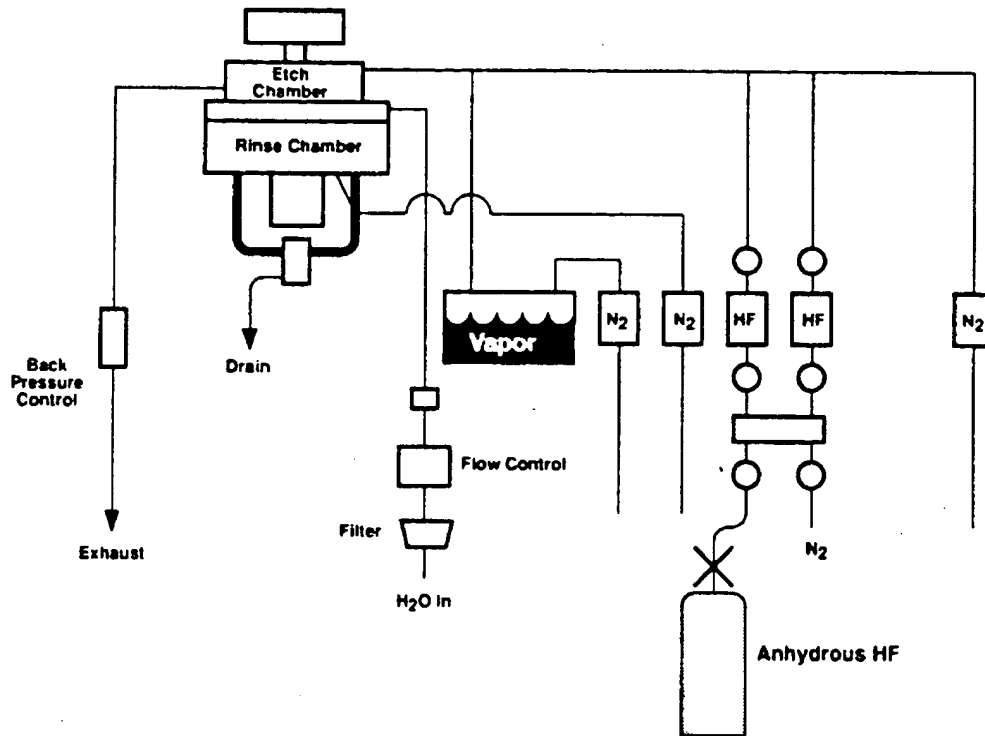
Subsequent product improvements have included the addition of anhydrous HCl for enhanced metallic contamination removal, ozone gas for light organic cleaning and re-oxidation of silicon, a nitrogen ambient wafer staging area and loadlock capability for downstream processes.

Applications for the FSI system have included silicide cleaning, pre-gate cleans including the etching of the sacrificial oxide before gate

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\*Excalibur is a registered trademark of FSI International.

oxidation, and pre-metal contact cleans, especially where CVD technology was chosen over PVD for first level metal contacts. Additional applications include pre-epi and pre-polysilicon deposition cleans and bond pad etching.



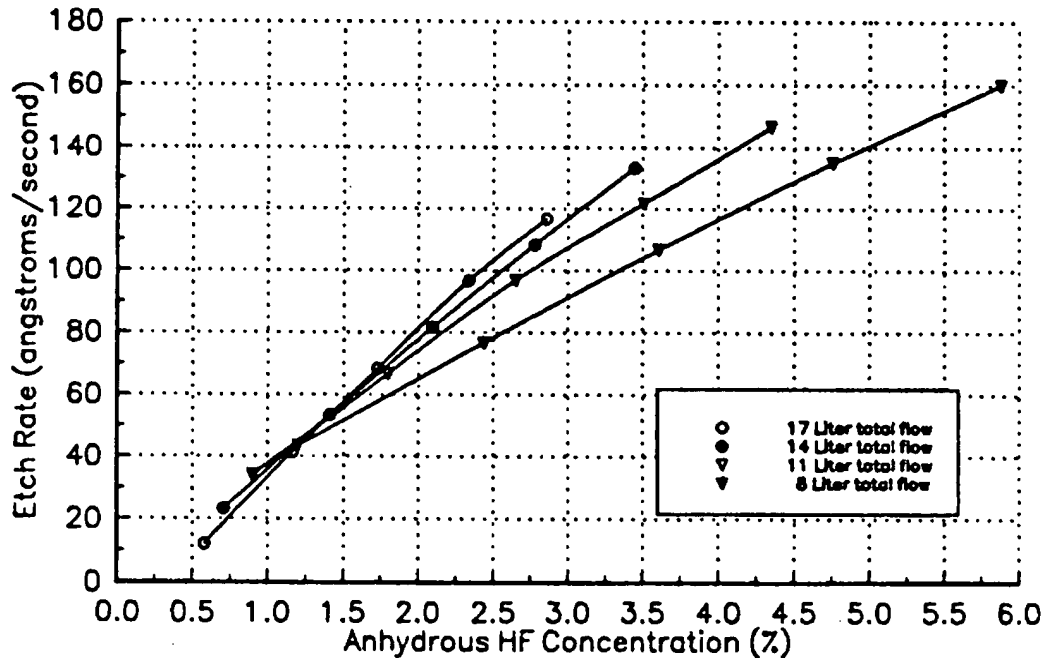
**Figure 4.** Schematic of Excalibur integrated vapor etch/rinse system. (Courtesy of FSI International).

Controlled etch rates can vary from 1 to 300 Å/second with total one sigma uniformity of  $\pm 2\%$ , within wafer, wafer to wafer and batch to batch on a 200 Å etch of thermal oxide. The system is particle neutral at sizes equal to or greater than 0.2  $\mu\text{m}$ . Oxide etch rates as a function of anhydrous HF concentration for various total flow rates are shown in Fig. 5.

**Vapor Phase Reactants.** Another type of wafer cleaning system involves *vapor phase* chemistries and was originally based on the vaporization of azeotropic mixtures of hydrogen fluoride and/or hydrogen chloride and water vapor (59)(60). This system is manufactured by Advantage Production Technology, Inc.; a schematic of the initial model (EDGE-2000) is shown in Fig. 6. The chamber of this system is about the size of a basketball and is constructed of a specially formulated silicon carbide material by Norton Co. (61). It consists of two hemispheres and a center ring. It will accommodate one wafer, up to 200 mm in diameter, positioned vertically. Gases are admitted through one side and evacuated from the



other. In the first model, wafers were maintained at room temperature (22° - 25°C) but in later versions, higher wafer temperatures were employed (see below).



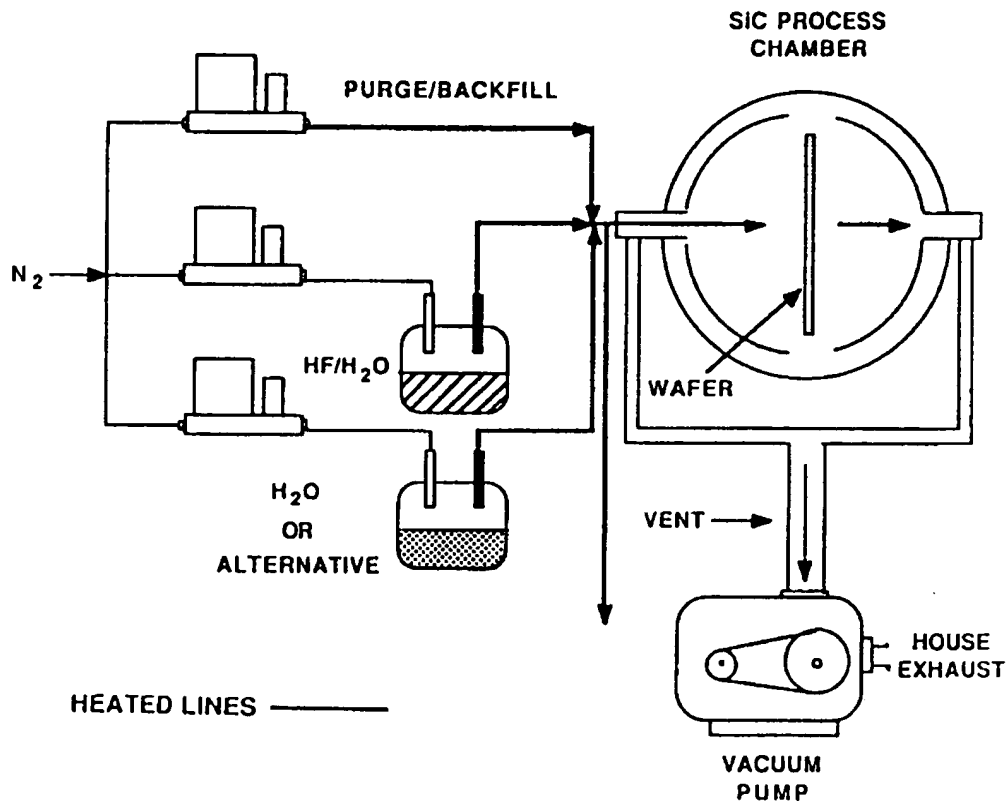
**Figure 5.** Thermal oxide etch rate versus anhydrous HF concentration at 25°C for various total flow rates in the Excalibur wafer cleaning system. (Courtesy of FSI International).

Vaporizers, shown in Fig. 6, can contain solutions of HF/H<sub>2</sub>O, HCl/H<sub>2</sub>O, H<sub>2</sub>O, or various solvents such as CH<sub>3</sub>OH. The solutions are heated to appropriate temperatures to provide various vapor pressures of the reactants. Vapors of these reactants are transported to the chamber by inert gases such as nitrogen or argon, whose flow rates are controlled by mass flow controllers. All materials in contact with the acids (HF, HCl, etc.) are silicon carbide or Teflon\* based.

Also shown in Fig. 6 is a vacuum pump which permits the system to be evacuated to the low mtorr range. Thus, vapor phase cleaning and etching processes can be carried out at reduced pressure which assists in vaporization of reactants, reaction products, and contaminants. A typical cleaning sequence is indicated in Fig. 7, where a pressure-time cycle is shown. At the start of the cycle, the wafer is automatically inserted into the

\*Teflon is a registered trademark of Dupont.

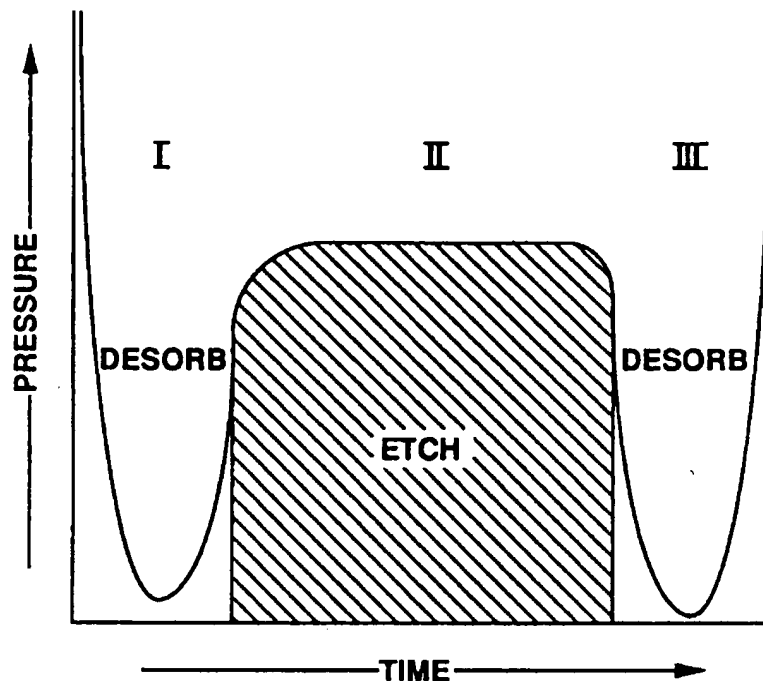
chamber, the door is closed, and the chamber evacuated to about 1 torr for a few seconds (I). Reactant gases are then admitted to the chamber to pressures ranging from 100 to 400 torr for times of 10 to 60 seconds (II). The system is then again evacuated to the low mtorr range for a few seconds (III), after which  $N_2$  or Ar is readmitted to the chamber. As noted in a following section, the final evacuation or desorb step dries the wafer and no further drying is necessary. This overall cycle may be varied and is programmed and controlled by computer.



**Figure 6.** Schematic of Advantage Production Technology's EDGE-2000 vapor phase wafer cleaning/etching system; after Deal et al. (60). Note: Technology of Advantage presented by Genus, Inc. in 1992.

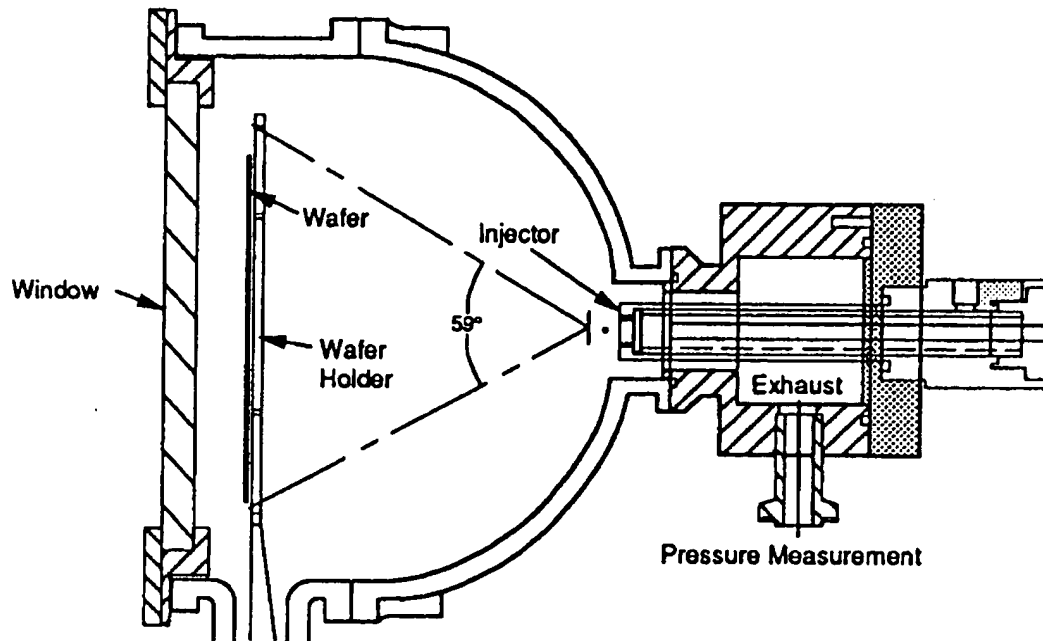
A more advanced model of the Advantage vapor phase cleaning system employs wafer heating and ozone activation (model EDGE-2002). A cross section of the process chamber is shown in Fig. 8. In this system, the silicon carbide chamber has been modified and consists of a single hemisphere with a flat quartz window across the diameter. This window or plate is covered by a special transparent material that resists attack of the quartz by hydrofluoric acid. The wafer can be exposed to IR (or UV) for

heating up to 400°C. In addition, a corona discharge ozone source is connected to the inlet lines so that ozone may be admitted to the chamber before or during the clean/etch treatment cycle. It has been found that pretreatment of oxide surfaces using ozone at elevated temperatures is a very effective treatment for removing deposited hydrocarbons, and much more uniform etching of silicon oxides can be achieved (62).



**Figure 7.** Pressure versus time characteristic of EDGE-2000 vapor phase oxide etching process; after Deal et al. (60).

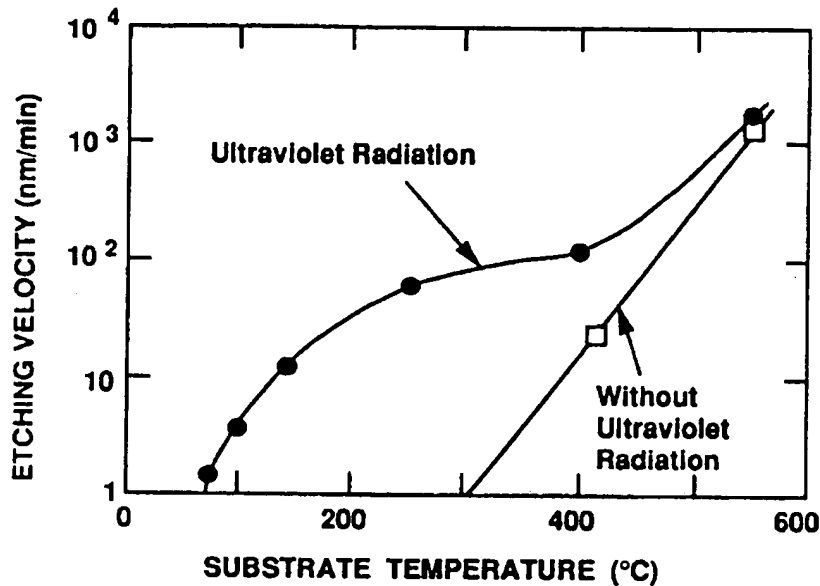
Vapor phase cleaning and etching has been shown to eliminate many of the particle contamination problems discussed above which have been associated with aqueous-type cleaning processes. In general few, if any, particles are added during vapor phase processes, and often particles are actually removed. It is anticipated that in situ particle monitoring can be employed in more advanced systems (described later). It is also possible to employ other in situ monitoring tools, such as residual gas analyzers (RGA), ellipsometers, and in-line particle counters. Other experiments involving vapor phase HF processing, along with appropriate equipment, have been reported by van der Heide et al. (63), Onishi, Oki, and co-workers (54)(64)(65), Wong et al. (66)(67), and by Izumi and co-workers (68).



**Figure 8.** Modified process chamber of EDGE-2002 vapor cleaning system which permits UV/IR radiation of wafer through passivated quartz window at left. (Courtesy of Advantage Production Technology).

**Activated Chlorine.** While the use of activated chlorine gas for cleaning silicon wafers has not been developed to the point of commercial application, it is probably the most likely to be used in wafer production after HF vapor cleaning and etching. It was mentioned earlier that vapor HCl has been successfully used for a number of years as a pre-epitaxial silicon deposition step for removing native oxides and other contamination. It has since been reported by researchers at Fujitsu and others that the use of activated chlorine ( $\text{Cl}_2$ ) gas can be an effective method for removing metal impurities from the silicon surface (69)-(74).

Most of the work in this area has involved ultraviolet activation of chlorine gas (70)-(74). The mechanism involves etching and removing a thin layer of silicon which either vaporizes the metal atoms as  $\text{MCl}_x$  along with the silicon, or by lifting the metal on top of the evaporating silicon chloride. Typically, UV light in the 180 to 350 nm wavelength range is used at temperatures from 100 to 400°C. In Fig. 9, the relationship of silicon removal rate to substrate temperature for  $\text{Cl}_2$  with and without UV radiation is shown (75). The main challenge in establishing a production-worthy process is the control of the silicon etch rate so that a minimum but uniform layer is removed.



**Figure 9.** Photochemical etching of silicon wafer by chlorine gas with and without ultraviolet radiation; after Ito et al. (75).

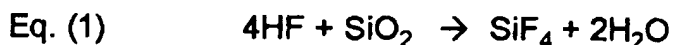
A second type of  $\text{Cl}_2$ -activated etching of silicon has been reported using a downstream microwave discharge system (76). The authors investigated effects of various process variables, such as silicon orientations, doping concentration, and substrate temperature. As was the case for UV activation, the main problem in this type of cleaning process is the ability to uniformly etch the silicon. This will be a requirement for submicrometer device fabrication, but hopefully these uniformity problems will be solved. The current effectiveness of activated chlorine treatment for metal impurity removal is discussed in Sec. 5.5.

### 3.0 OXIDE ETCHING

#### 3.1 Thermal Oxides

One of the more critical steps in semiconductor device fabrication is the complete or partial thickness removal of thermal oxide layers from the wafer surface. This removal or etching must be accomplished uniformly across the wafer or in selected regions. Typically, oxides are etched in hydrofluoric acid aqueous solutions. It is therefore appropriate to first mention aqueous etching processes. These etch processes are typically

carried out by immersing a batch of wafers in a bath containing the etch solution. Appropriate temperature control and stirring are employed to maintain constant and uniform etch rate conditions. The overall chemistry may be expressed by one of the following reactions:



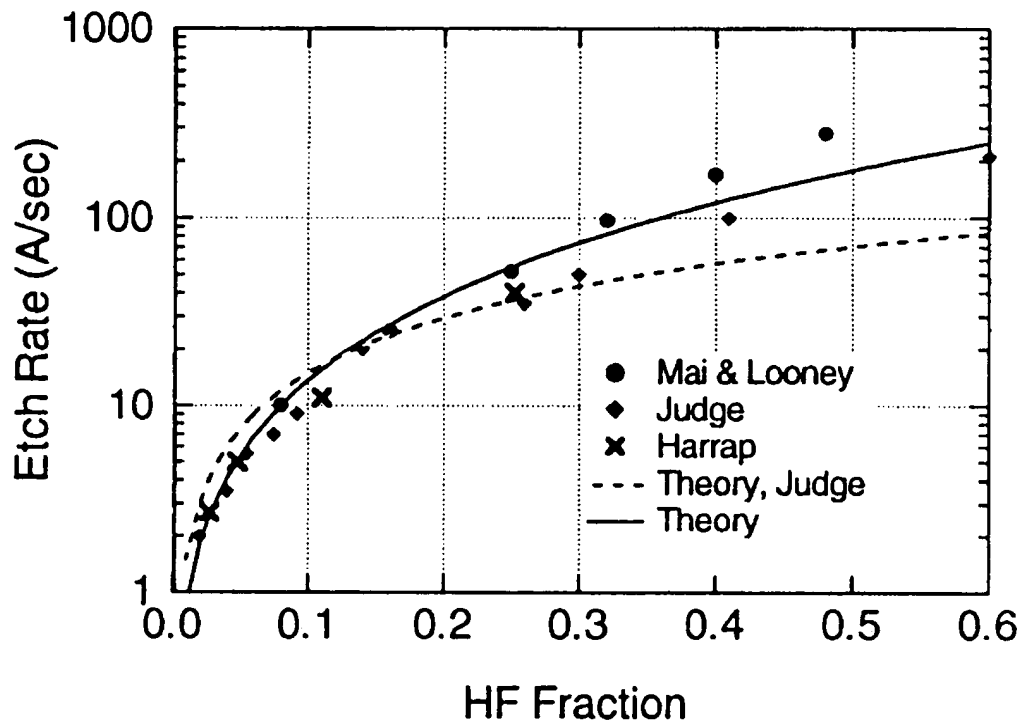
In any such reactions, various intermediate species are produced, and Eqs. (1) or (2) are no exception. These intermediates can cause problems either during the oxide etching process or afterwards, and the subject is discussed in the following section which deals with oxide etching mechanisms.

Unfortunately, very few data concerning aqueous HF-H<sub>2</sub>O etching exist in the literature, since most of these procedures involve so-called buffered oxide etch solutions. In this case, mixtures of ammonium fluoride and hydrofluoric acid (NH<sub>4</sub>F + HF + H<sub>2</sub>O) are generally used, which tend to prevent depletion of the fluoride ions—thus leading to stable etch characteristics (77). Other additives, such as glycerol are sometimes used as well.

Some early references by Mai and Looney (78), Judge (79), and Harrap (80), which provide thermal oxide etch rate data in HF-H<sub>2</sub>O mixtures, are available, and these have been used to prepare the plot shown in Fig. 10. This plot will be used later to compare vapor phase HF etching of thermal oxides with aqueous etching. Etch rates are normally obtained by plotting oxide removed versus etch time for a particular set of process conditions. The etch rate is determined from the slope of the curve.

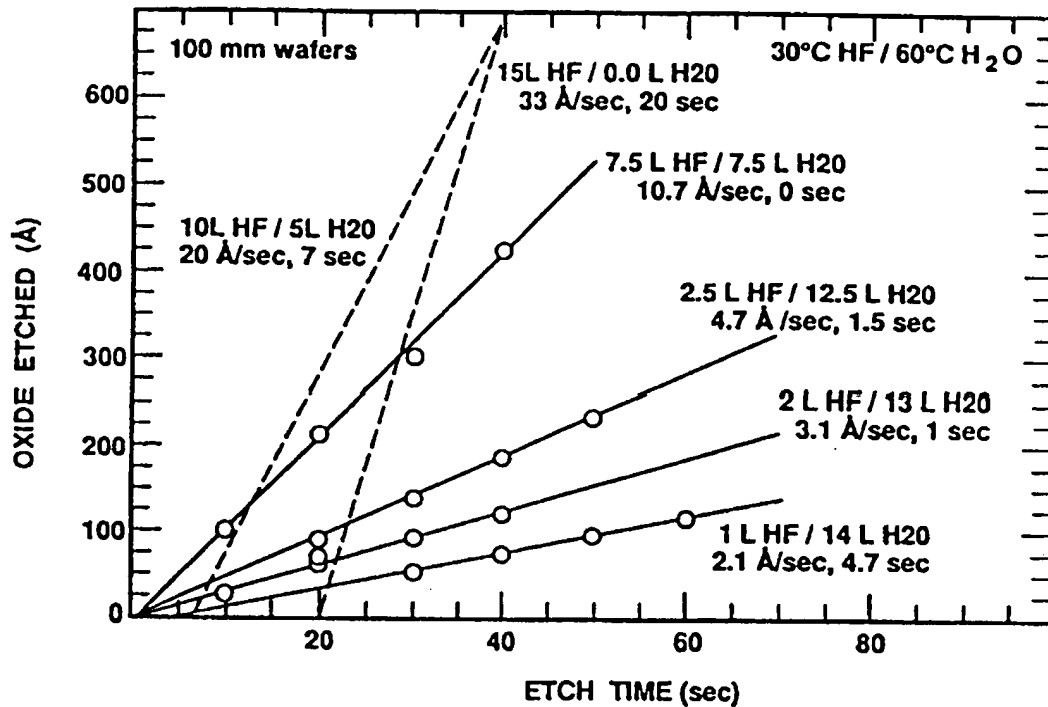
In vapor phase HF etching of oxides, an interesting phenomenon has been observed. While the process occurs as indicated in Eqs. (1) or (2), etching does not begin without the presence of condensed water on the oxide surface. The mechanism is discussed in detail in the next main section. Needless to say, the nature of the etch process is very dependent on the chemistry of the oxide surface and the effect on the water condensation. Variations in this chemistry will result in differences in delay time, that is, the on-set of etching. Once etching of the oxide does begin, it tends to be linear with time. Etch rate values are functions of HF concentration in the condensed aqueous layer, which in turn are dependent on temperature, pressure, and other process variables. A typical example of oxide etch rate plots is presented in Fig. 11. Normally, these types of measurements

of oxide thickness removed during a particular etch time are carried out using suitable mapping equipment such as a Prometrix model SM 200/e, or a Gaertner model L115B. The variation of delay or off-set times with HF concentration in the vapor phase can be observed in Fig. 11, along with etch rates themselves. An estimation of HF concentration in the condensed aqueous layer for particular HF:H<sub>2</sub>O vapor ratios can be made by comparing etch rates with those of Fig. 10 for aqueous solutions. For instance, a 4.7 Å/sec etch rate obtained by vapor etching with a 2.5 l/min azeotropic HF source and 12.5 l/min H<sub>2</sub>O source corresponds to about a 5 wt% HF aqueous solution.



**Figure 10.** Thermal oxide etch rate as a function of HF concentration (wt.%) in aqueous HF solutions at 25°C. The data are from Refs. 78, 79, and 80. The dashed line is from Judge; the solid line is an improved fit discussed in Sec. 4.2.

In partially etching blanket oxide layers or selectively etching oxides, it is generally very important to etch as uniformly as possible. Good etch uniformity is important across the wafer as well as from wafer to wafer (often called repeatability). Typical data reported for the Advantage EDGE-2000 system are summarized in Table 1. Note that oxide etching uniformity and repeatability values are for clean oxides.



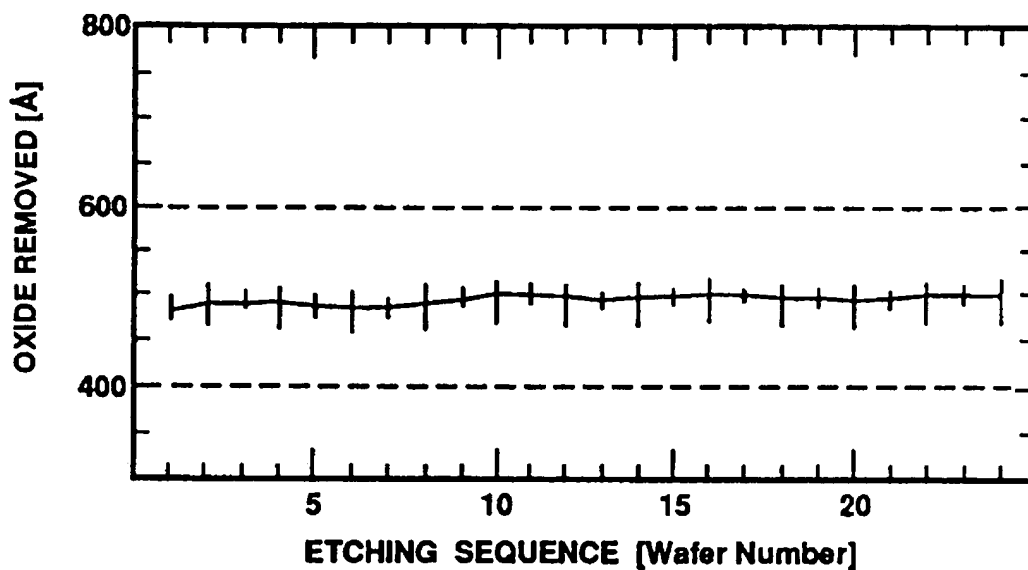
**Figure 11.** The amount of thermal oxide removed versus etch time for varying ratios of azeotropic HF/H<sub>2</sub>O solutions (38.4 wt.% HF) to water vapor. The wafer temperature is 25°C, the azeotropic HF/H<sub>2</sub>O vaporizer temperature is 30°C, and the water vaporizer temperature is 60°C. The total flow rate is 15 l/min. The etch rate equals the slope of plots (first number, second line); the delay time equals the time intercept (second number, second line); after Deal et al. (60).

**Table 1.** Typical Properties: Vapor Phase Oxide Etch Process  
(150 mm wafer, 22°C)

■ ETCH RATES - THERMAL OXIDES	
AZEO HF	30 - 70 Å/sec
HF - H <sub>2</sub> O	2 - 35
HF - HCl	5 - 25
HF - IPA	0.2 - 5
■ ETCH UNIFORMITY - THERMAL OXIDES	
≤2.0% (one sigma)	
■ ETCH REPEATABILITY - THERMAL OXIDES	
≤3.0% (one sigma)	
■ PARTICLE ADDITION (bare wafer)	
≥0.4 μm	0 - 2
≥0.2 μm	3 - 10



The effect of organic impurities on the oxide surfaces or even the surface chemistry itself on oxide etch characteristics, especially for vapor etch systems, has already been mentioned. Data have been obtained which demonstrate this effect (62) and are shown in Fig. 12. This evaluation was carried out in the Advantage System 2002 which includes wafer heating and ozone capabilities. A single lot of twenty-four oxidized silicon wafers were selected and every other wafer was given an ozone pre-etch treatment at 200°C. All wafers were then vapor etched in HF-H<sub>2</sub>O to remove 500 Å oxide. A distinct improvement in oxide etch uniformity was observed for the ozone pre-treated wafers, confirming that even for relatively clean oxides, enough organic contamination is present on the oxide surface to affect etching uniformity. On the other hand, etch repeatability from wafer to wafer is not affected appreciably.



	<u>Uniformity (1 sigma)</u>	<u>Repeatability (1 sigma)</u>
Pre-etch Treat.	0.90%	1.04% (1.31%)
No Pre-etch Treat.	2.17%	0.92%

**Note: Odd wafer numbers have ozone+heat pre-treatment**

**Figure 12.** Uniformity of thermal oxide etching in vapor phase cleaning system with and without an in situ ozone/heat preclean; after Nobinger et al. (62).

As mentioned earlier, other process variables which can significantly affect vapor phase oxide etch characteristics include wafer temperature, chamber pressure, and any variable affecting composition of the condensed HF aqueous layer, such as gas flow rates, vaporizer composition and temperature, and type of solvent. The latter effect on etch rates is indicated in the first part of Table 1 where several solvents are listed.

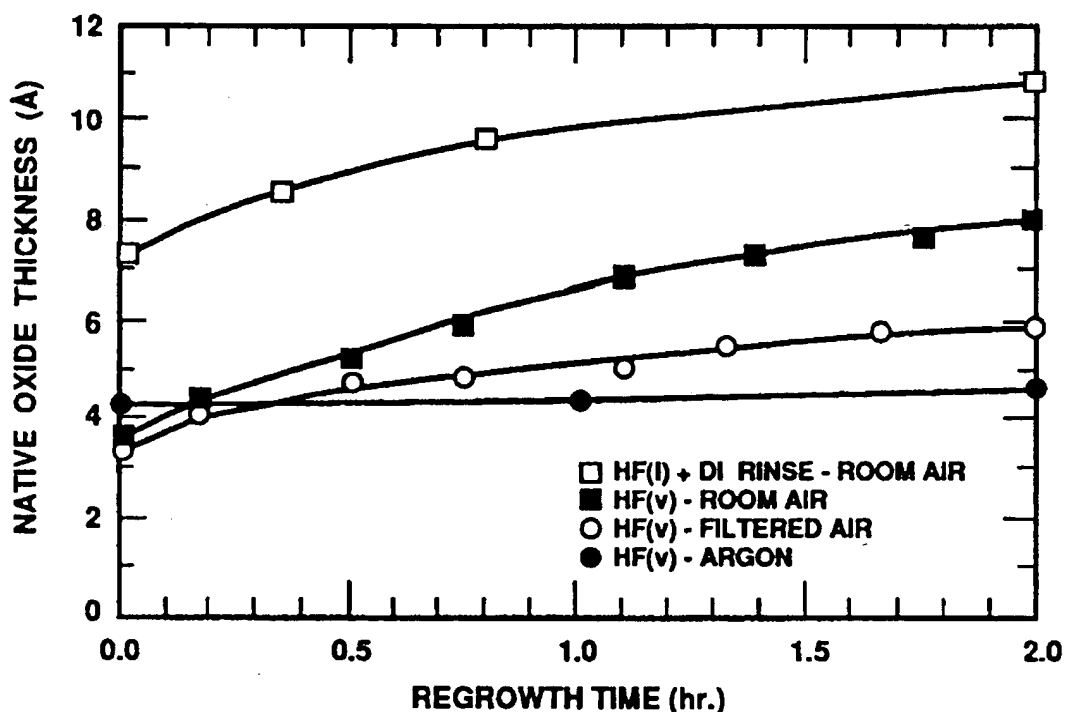
### 3.2 Native/Chemical Oxides

Perhaps a great majority of applications involving vapor phase HF etching of oxides relate to complete removal of a thick (or thin) oxide. After this removal, and after various cleaning treatments of "stripped" silicon surfaces, a thin (5 - 15 Å) oxide layer generally remains. Thus, the important subject of so-called "native" or "chemical" oxides arises, including native oxide regrowth (81)-(87). Many device structures are critically affected by the presence or absence of this thin layer of questionable composition. These structures include interconnect contacts, poly-Si bipolar emitters, epitaxial silicon layers, and even MOS gate oxides. Practical aspects of pre-cleaning effects on device properties are discussed in a later section.

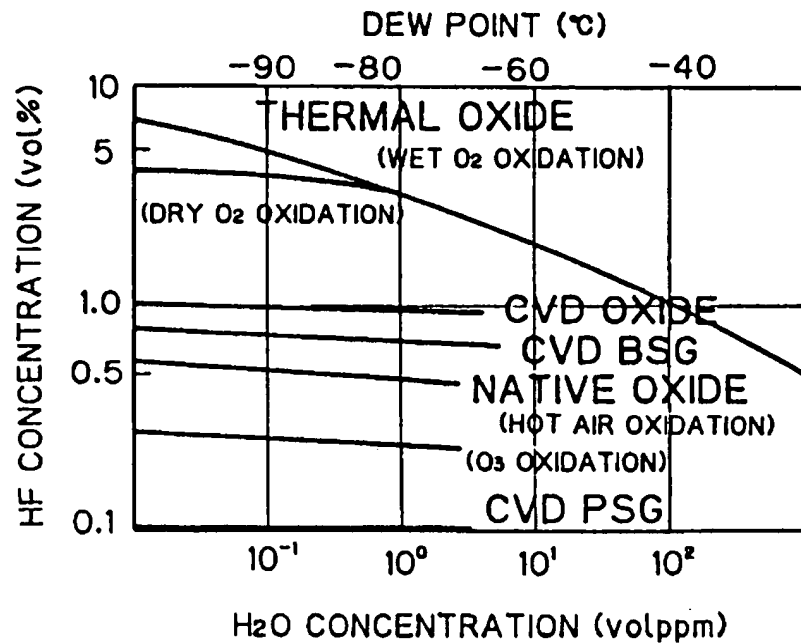
As mentioned above, any subsequent treatment of an HF-etched silicon surface will normally result in the formation of a very thin native or chemical oxide. This treatment can include cleaning solutions, DI water, process gases, or even exposure to room ambient. These layers vary in composition, depending on the treatment, but quite often contain silicon oxide, organics, various anions such as sulfates, and other impurities. Thus it has been very difficult to characterize them and to obtain reproducible evaluations in different laboratories. Various techniques have been used to determine their thickness and composition, such as XPS, Auger, SIMS, and ellipsometry. Kinetics of film growth have been investigated and typical results are presented in Fig. 13. In this figure, it can be noted that after a conventional aqueous HF etch and DI water rinse, the apparent native oxide thickness is 7 - 8 Å. For a vapor phase HF treatment, however, the thickness is about 4 Å for this particular substrate, as measured by an ellipsometer. If both wafers are exposed to room ambient, a steady thickness increase is observed. On the other hand, the increase is much less for exposure to either charcoal filtered air or argon. This has led to the conclusion that much of the so-called re-oxidation is really due to a condensation of organic and other impurities on the surface (62)(88).

One of the device fabrication requirements in removing native/chemical oxides from contact openings is that attack of the surrounding dielectric should be minimal. Ideally it should not be etched at all. It has

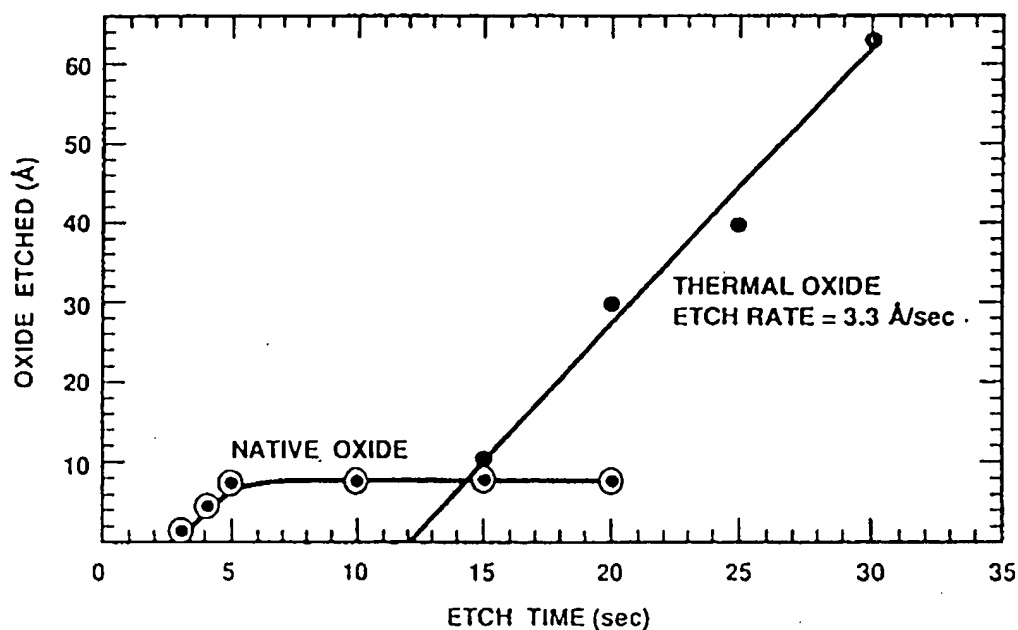
been found by groups at the Hashimoto Chemical Industries and Tohoku University that extremely dry anhydrous HF can remove native oxide layers without etching adjacent thermal oxides (89). In their work, a vapor phase HF critical concentration was found below which no etching was observed. This critical concentration depended on residual  $\text{H}_2\text{O}$  present, temperature, and flow rate, as well as the nature of the  $\text{SiO}_2$  being etched. They suggested that, indeed, water was necessary for etching to proceed and that hydrated surfaces, such as chemical native oxides would therefore have lower HF partial pressure thresholds; whereas drier surfaces, such as thermal oxides, would have higher thresholds. Once the reaction is initiated at sufficiently high HF pressures, enough water will be produced to allow the reaction to continue. Data which demonstrate such selective oxide etching are presented in Fig. 14. It has also been observed that a similar selective etch process can be achieved using the vapor HF- $\text{H}_2\text{O}$  reaction. This is accomplished for those conditions which produce a delay time of 10 seconds or more before etching of the thermal oxide begins. Since the condensed aqueous HF solution has not yet formed, the gaseous HF will etch the native oxide but not the thermal oxide. This phenomenon is illustrated in Fig. 15, where an 8 Å native oxide is removed before etching of the thermal oxide commences.



**Figure 13.** Native oxide regrowth at 25°C in various ambients following vapor and liquid HF strip of thermal oxide.



**Figure 14.** Relationship of HF critical concentration (for oxide etching) and moisture level at 25°C for various dielectric films. Native oxides were prepared by hot air and ozone oxidation; after Miki et al. (89). (Copyright 1990, IEEE).



**Figure 15.** Selective etching of native oxides in presence of thermal oxides using vapor phase HF processes.

### 3.3 Deposited Oxides

Various types of dielectric films, usually based on  $\text{SiO}_2$ , are used in semiconductor device fabrication (18)(90)(91). These can be deposited by a variety of methods and may contain dopants, such as phosphorus and boron, in amounts up to 10%. As a result, etch rates can vary considerably. For a given etch process, aqueous or vapor, each film must be characterized. In addition, when two or more dielectrics are present on the same wafer, differential etch rates are often observed. Many times, etch rate differences can be used to advantage for fabricating a particular device, while in other cases severe problems result. In Table 2, examples of relative etch amounts for different dielectric films are shown for a given etch time in a vapor phase  $\text{HF}/\text{H}_2\text{O}$  system.

Similar data have been repeated for other vapor etch systems; an example is shown in Fig. 16. Note that etch rate increases with increasing dopant concentration and/or lower density deposited films.

**Table 2.** Relative Etch Selectivity of Various Thin Films  
(45°C HF Vaporizer; 12 sec. etch time)

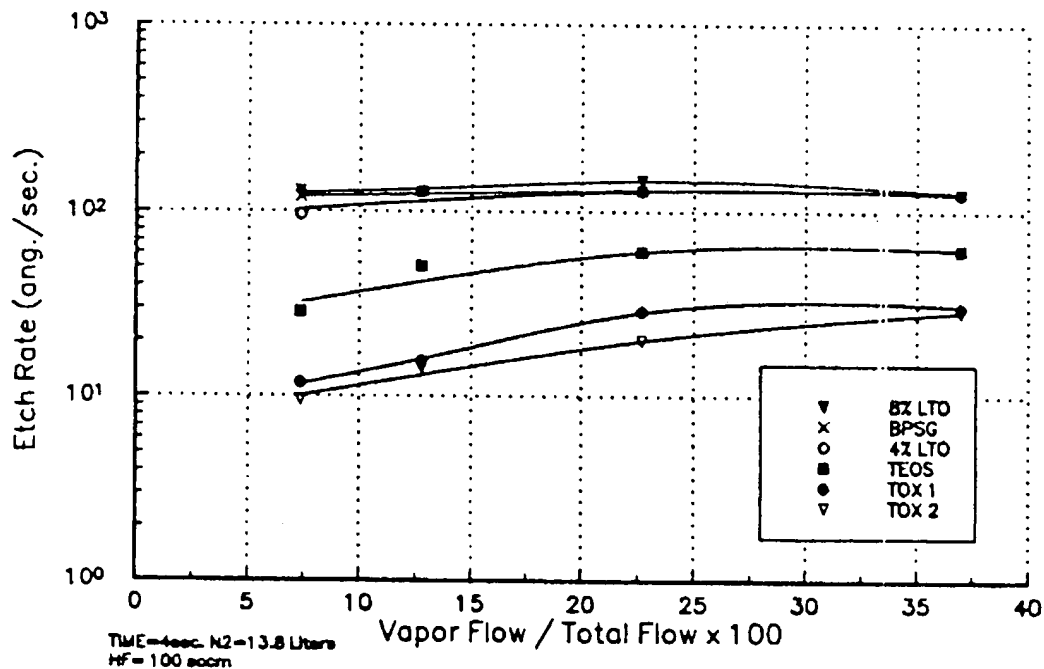
Oxides	Thickness Etched	Selectivity (Compared to Thermal)
Thermal	240 Å	1.0
LTO	360 Å	1.5
TEOS	550 Å	2.1
PSG (4% P)	776 Å	3.2
BPSG (4% B, 7%P)	1288 Å	5.4

## 4.0 MECHANISM OF OXIDE ETCHING

### 4.1 Background

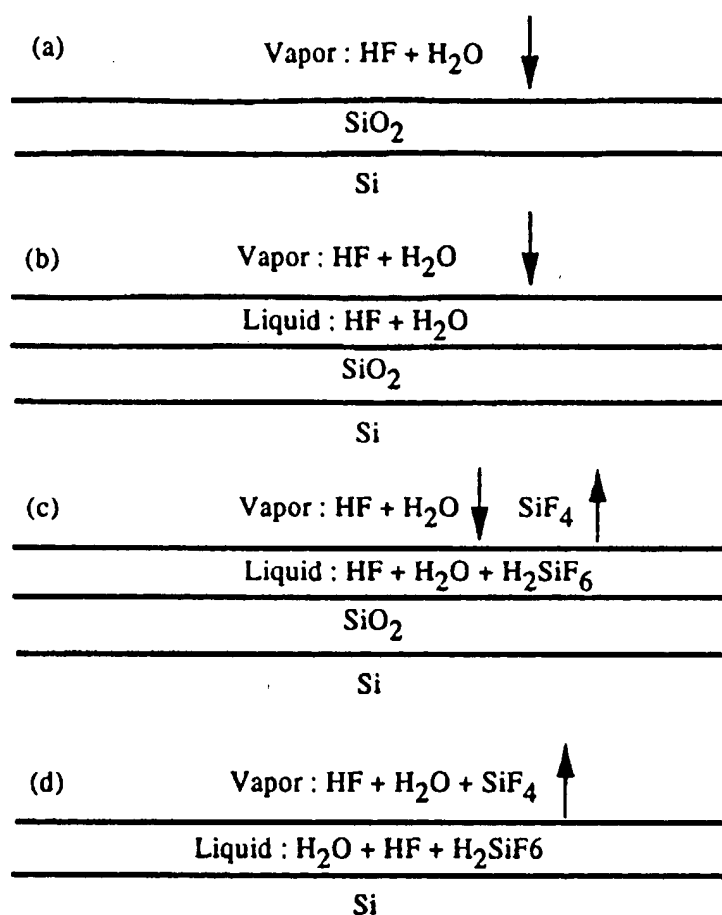
In our work on oxide cleaning and etching (37)-(39) we have taken the lead from the Holmes & Snell (36) work in light of subsequent data to develop a quantitative model of vapor phase  $\text{HF}/\text{H}_2\text{O}$  etching of  $\text{SiO}_2$ . The basis of the model is the initial assumption that etching will only proceed if

a condensed HF-containing liquid layer is present on the surface. There is a significant amount of evidence in support of this assumption. An example is shown in a comparison of vapor phase etch rates illustrated in Figs. 5 and 11 with what is obtained in aqueous solutions as shown in Fig. 10. In both cases the ranges of etch rates are similar, suggesting similar mechanisms. In another example the thresholds in etching observed (see Figs. 2 and 14) for the vapor phase can be quite naturally related to the requirement for condensation for etching to occur. A major part of the model is therefore determining those conditions of temperature, HF, and  $H_2O$  partial pressures that lead to condensation. Proceeding on the assumption that etching then occurs in the same way as for liquid solutions, a steady state model allows the calculation of the HF concentration in the condensed liquid film. A comparison of that value to the liquid case then permits the vapor phase etch rate to be determined. This model has provided excellent agreement with experiment including the observations of etching selectivity, pressure and temperature thresholds, and induction times reported by numerous investigators.



**Figure 16.** Etch rates at 25°C versus  $H_2/N_2$  vapor flow for various dielectric films in Excalibur vapor cleaning system (Courtesy of FSI International).

A schematic of how this process works is shown in Fig. 17. Initially an  $\text{SiO}_2$  surface is exposed to a vapor phase mixture of  $\text{H}_2\text{O}$  and  $\text{HF}$  (17a). If the partial pressures are sufficient, then a condensed film of  $\text{HF}$  and  $\text{H}_2\text{O}$  will form and continue to grow on the  $\text{SiO}_2$  surface (17b). Etching proceeds with the formation of  $\text{H}_2\text{SiF}_6$  and additional water (17c). Although the partial pressure of  $\text{SiF}_4$  over dilute  $\text{H}_2\text{SiF}_6/\text{HF}/\text{H}_2\text{O}$  solutions is relatively low, some  $\text{SiF}_4$  will evolve during the etching process. When the etching is complete and the  $\text{HF}$  and  $\text{H}_2\text{O}$  reactants are switched off, the liquid  $\text{H}_2\text{SiF}_6/\text{HF}/\text{H}_2\text{O}$  film can be evaporated (17d) or rinsed off.



**Figure 17.** Schematic diagram of the various steps occurring during the etching of  $\text{SiO}_2$ .

## 4.2 Important Aqueous Chemistry

The chemistry of vapor phase  $\text{HF}$  or  $\text{HF}/\text{H}_2\text{O}$  etching or cleaning of  $\text{SiO}_2$  on  $\text{Si}$  is closely related to the aqueous analog and is reviewed to

provide a complete discussion of the vapor phase case. The chemistry of these processes has been discussed by Judge (79) and more recently by the Hashimoto/Tohoku University groups (92). In addition to a review of these works, additional information related to the effect of cleaning chemistry on surface roughness has been forthcoming (93).

**The Chemistry of HF Etching of SiO<sub>2</sub>.** The overall chemistry of the etching process is described by Eqs. (1) and (2). However the properties of HF/H<sub>2</sub>O mixtures are complicated due to the incomplete ionization of the HF and the formation of more complex species such as HF<sub>2</sub><sup>-</sup>. Previous studies (79) have established the equilibrium for these species via

$$\text{Eq. (3)} \quad [\text{H}^+][\text{F}^-] = K_1[\text{HF}]$$

and

$$\text{Eq. (4)} \quad [\text{HF}][\text{F}^-] = K_2[\text{HF}_2^-]$$

giving values for  $K_1$  and  $K_2$  of  $1.3 \times 10^{-3}$  and 0.104 at 25°C, respectively. The corresponding concentration of the various species as a function of total HF concentration is shown in Fig. 18. Note the pH corresponds to the  $\log[\text{H}^+]$  which can be obtained from the left hand axis. From the perspective of SiO<sub>2</sub> etching, the question is, Which of these species are active? Two species  $\text{H}^+$  and  $\text{F}^-$  are clearly inactive. We conclude this since other acids with high  $[\text{H}^+]$  don't etch SiO<sub>2</sub> and pure NH<sub>4</sub>F with a high  $[\text{F}^-]$  also doesn't etch SiO<sub>2</sub>. That leaves the HF and HF<sub>2</sub><sup>-</sup> species. Tests of the activity of these species have been made by adjusting the ion concentrations in HF solutions using either HCl or NH<sub>4</sub>F. For high HCl concentrations very little  $\text{F}^-$  or HF<sub>2</sub><sup>-</sup> are present so the etching occurs primarily due to the neutral HF. For high NH<sub>4</sub>F concentrations very little  $\text{H}^+$  or neutral HF is present so the etching occurs primarily due to the HF<sub>2</sub><sup>-</sup>. This is shown in Fig. 19 where the HF/HF<sub>2</sub><sup>-</sup> concentration ratio is plotted versus HF concentration for the case of pure HF/H<sub>2</sub>O and cases of HCl and NH<sub>4</sub>F additions. Indeed, significant etch rates are found for both cases, indicating that there is significant activity for both HF<sub>2</sub><sup>-</sup> and neutral HF. Judge (79) deduced a fit to much of his data as

$$\text{Eq. (5)} \quad \text{Etch Rate (25°C)} = 2.5[\text{HF}] + 9.7[\text{HF}_2^-] - 0.14$$

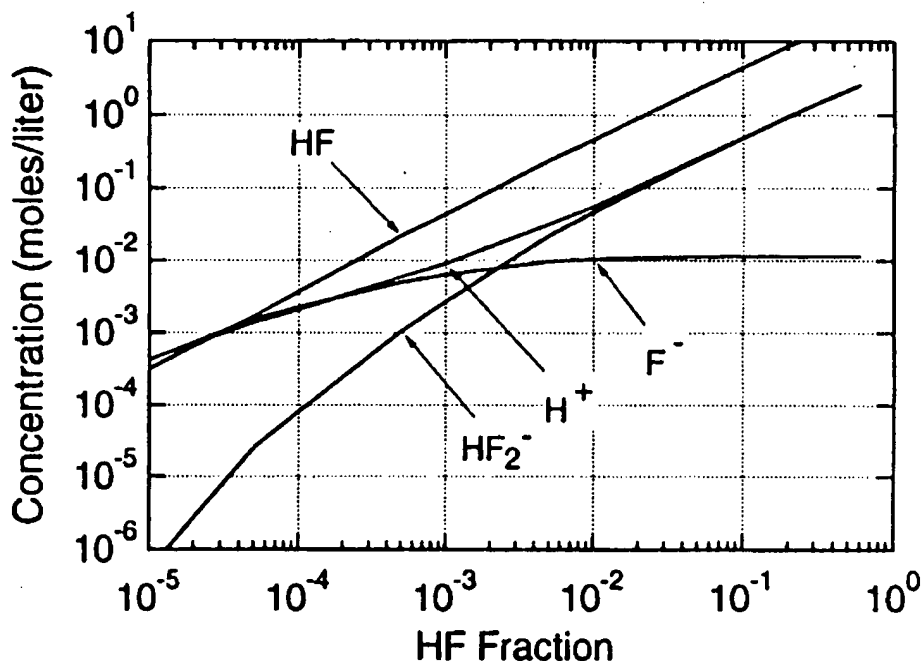
indicating that the HF<sub>2</sub><sup>-</sup> is considerably more active for SiO<sub>2</sub> etching than HF. This explains the high etch rates observed for buffered HF solutions with high  $\text{F}^-$  and therefore HF<sub>2</sub><sup>-</sup> concentrations. Although the above relationship works well for some conditions it is not accurate for high HF



concentration cases of interest for vapor phase etching. This is shown in Fig. 10 where Eq. (5) is shown as the dotted line. The fit is clearly poor, especially for the high concentration limit, and in addition, a negative term in Eq. (5) is not physically meaningful. A better fit can be obtained if a term in  $[\text{HF}]^2$  or  $[\text{HF}_2^-]^2$  is added. The solid line fit of Fig. 10 corresponds to:

$$\text{Eq. (6)} \quad \text{Etch Rate (25°C)} = [\text{HF}] + 7[\text{HF}_2^-] + 0.3[\text{HF}]^2$$

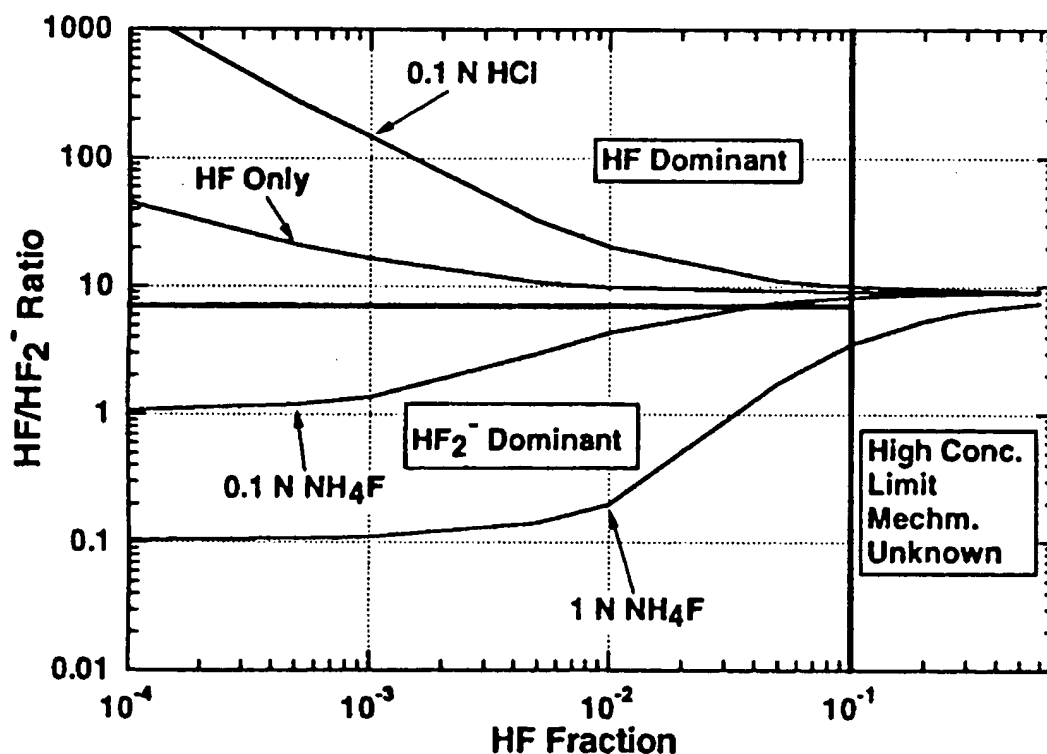
For a specific set of conditions the dominant reactant can be determined by calculating the relative magnitude in the above equation. This is also illustrated in Fig. 19.



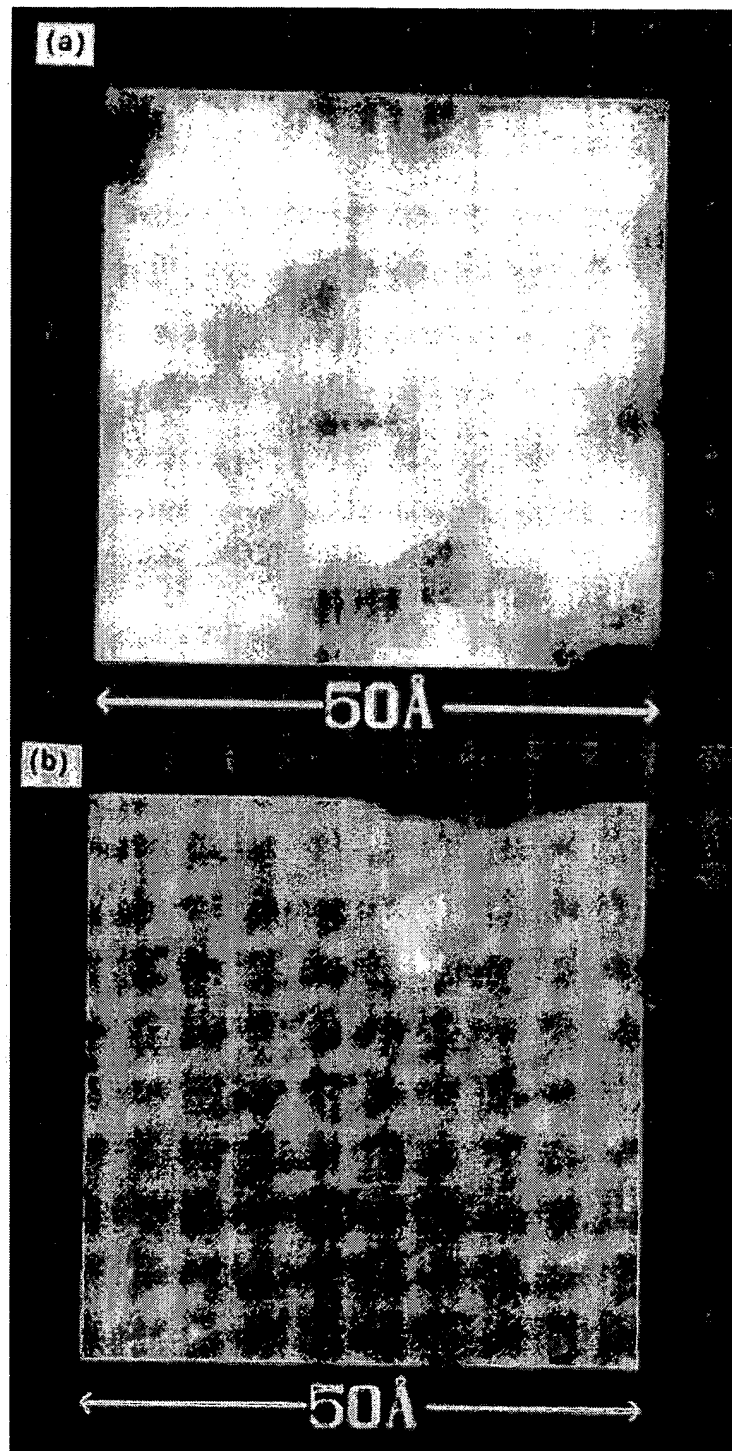
**Figure 18.** The concentration of various species is shown as a function of HF weight fraction from the model of Ref. 79. Note: the pH is the exponent of the  $\text{H}^+$  concentration.

**Surface Microroughness, Hydrogen Termination, and Electrical Implications.** These considerations may be thought to be of only academic interest. However, recent findings show that the pH of HF solutions effects the promotion of hydrogen-terminated surfaces and surface microroughness. It is now well appreciated that HF-last processing can lead to Si surfaces that are atomically clean except for a monolayer of hydrogen that terminates the Si dangling bonds (93)-(100). Surprising as it may seem, the surface concentration of fluorine is not seen to increase above 0.1 monolayer. Haring & Liehr (101) have shown that even Si surfaces fluorinated

in UHV are unstable in the presence of  $\text{H}_2\text{O}$  giving a surface where the Si is primarily bonded to oxygen and the remaining fluorine appears as OF radicals. Thus in an aqueous  $\text{H}_2\text{O}$  environment, fluorine terminated Si is clearly unstable. Both the low pH (HF dominated etching) and high pH ( $\text{HF}_2^-$  dominated etching) cases appear capable of producing these hydrogen-terminated surfaces. However, results from Higashi et al. (93)(100) show other differences between these two cases related to surface microroughness. This is shown in Fig. 20 where STM images of a low pH etched surface is shown in Fig. 20a and a high pH etched surface in Fig. 20b. The high pH case has led to a surface where the crystallinity is clearly evident, whereas the low pH case has produced a hydrogen-terminated surface which is considerably rougher. It is important to note that process induced surface microroughness has been correlated with poor interface and dielectric properties in MOS devices (102)-(110). In addition, cleaning induced microroughness has been attributed to less than ideal MOS properties for deposited  $\text{SiO}_2$  (111)-(113).



**Figure 19.** The  $\text{HF}/\text{HF}_2^-$  ratio plotted as a function of HF fraction for HF only, 0.1 normal HCl, 0.1 normal  $\text{NH}_4\text{F}$ , and 1 normal  $\text{NH}_4\text{F}$ .  $\text{SiO}_2$  etching will be dominated by HF for high ratios whereas it will be dominated by  $\text{HF}_2^-$  for low ratios, corresponding to  $\text{NH}_4\text{F}$  additions. For large HF fractions as encountered in vapor phase etching the important chemical mechanisms for  $\text{SiO}_2$  etching are unknown.



**Figure 20.** Scanning Tunneling Microscope (STM) images of Si(111) surfaces from Higashi et al. (93). Figure 20a shows a relatively rough surface morphology from low pH etching, whereas Fig. 20b shows a smooth morphology where atomic-scale features are resolved after a high pH ( $\text{NH}_4\text{F}$ ) etch.

Currently there is no vapor phase analog to  $\text{NH}_4\text{F}$  buffered HF, since  $\text{NH}_4\text{F}$  is not volatile and the use of  $\text{NH}_3$  with HF in the vapor phase will lead to  $\text{NH}_4\text{F}$  residues. Even though better device performance is expected for these HF/ $\text{NH}_4\text{F}$ -last surfaces, excellent device properties for vapor phase cleaned surfaces have been obtained, especially for HF/HCl-last surfaces, as discussed below.

### 4.3 Vapor Phase Mechanisms

For vapor phase etching we are interested in the comparison between measured liquid phase etch rates at a given HF concentration and the "vapor" phase etch rate at an identical calculated value of HF concentration in the condensed phase. We have shown that these etch rates are identical, validating the condensed film model (37)-(39). In addition, for vapor phase etching, the decomposition of aqueous  $\text{H}_2\text{SiF}_6$  via



with the desorption of  $\text{SiF}_4$  is a necessary step, unless a subsequent water rinse is employed. Undesired secondary reactions can cause residue formation not encountered in aqueous processing, as discussed below.

**Vapor Pressures of Aqueous HF/ $\text{H}_2\text{O}$  Mixtures.** In our previous work we have used the equilibrium partial pressures of HF and  $\text{H}_2\text{O}$  over aqueous solutions to determine conditions for condensation and HF concentrations which can then be used to determine etch rates. In this approach we assume that the system is in steady state with a flux of reactants into the surface (at sufficiently low pressures) given by

$$\text{Eq. (8)} \quad \Phi = P / (2\pi mkT)^{1/2}$$

where  $P$  is the pressure,  $m$  the mass, and  $kT$  the energy associated with temperature  $T$ . The flux of reactants leaving the surface is given by the appropriate reactant vapor pressures for the liquid phase. This is only valid if the sticking probabilities for the HF and  $\text{H}_2\text{O}$  are nearly equal; this is indeed the case, as shown below. Comparing masses we find that  $m_{\text{HF}} = 1.05 m_{\text{H}_2\text{O}}$  so assuming that the fluxes of each are proportional to their partial pressures leads to minimal layer error. For these conditions the net steady state flux into the condensed layer will be

$$\text{Eq. (9)} \quad \Phi_{\text{H}_2\text{O}} = P_{\text{H}_2\text{O}} - P_0^{\text{H}_2\text{O}}(T, [\text{HF}])$$

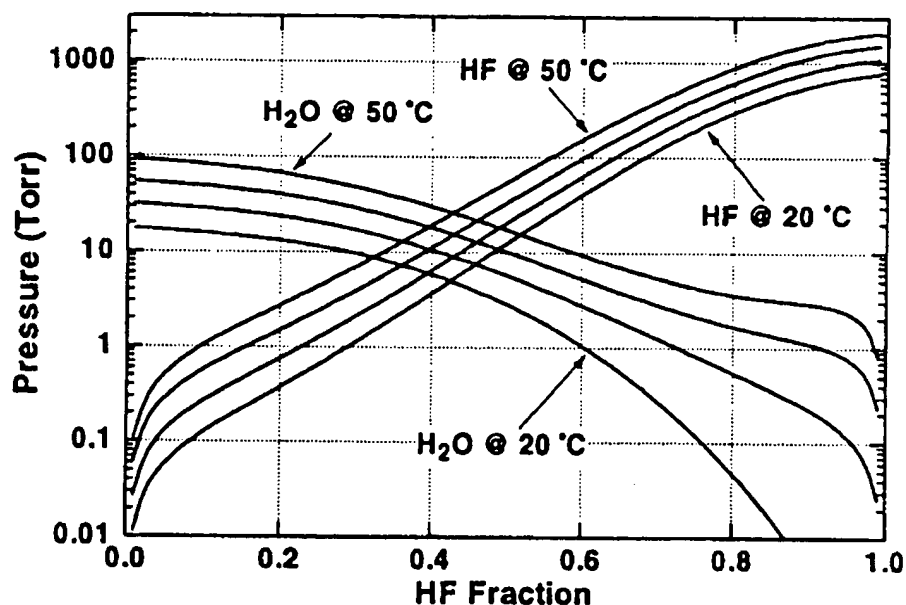
and

$$\text{Eq. (10)} \quad \Phi_{\text{HF}} = P_{\text{HF}} - P_0^{\text{HF}}(T, [\text{HF}])$$

where the  $\Phi$ 's are the fluxes,  $P$  is pressure,  $T$  surface temperature and  $[\text{HF}]$  is the HF concentration in the condensed layer.  $P_{\text{H}_2\text{O}}$  and  $P_{\text{HF}}$  are the vapor phase partial pressures right above the surface and  $P_0^{\text{H}_2\text{O}}$  and  $P_0^{\text{HF}}$  are the equilibrium vapor pressures at sample temperature  $T$  and condensed layer composition  $[\text{HF}]$ . The HF concentration in steady state is then determined by the ratio of the net HF flux to the total reactant flux, so that

$$\text{Eq. (11)} \quad [\text{HF}] = \frac{P_{\text{HF}} - P_0^{\text{HF}}(T, [\text{HF}])}{P_{\text{HF}} - P_0^{\text{HF}}(T, [\text{HF}]) + P_{\text{H}_2\text{O}} - P_0^{\text{H}_2\text{O}}(T, [\text{HF}])}$$

For a given set of experimental conditions this expression can be solved, providing values for the equilibrium vapor pressures are available. Fortunately there are extensive data in the literature on vapor/liquid equilibria for HF/H<sub>2</sub>O mixtures. The most complete reference on HF/H<sub>2</sub>O vapor/liquid equilibria appears to be that of Munter, Aepli and Kossatz (42); plots based on their data are shown in Fig. 21 where the equilibrium vapor pressures are plotted versus liquid composition for a series of temperatures including the values for pure HF. Additional recent data on the high HF concentration limit are also shown (114). Without further analysis we can make a few obvious statements from these curves. First, in the low HF concentration limit the vapor pressure of HF is quite small so that the HF fraction in the liquid phase will be much larger than in the vapor phase. The converse is true for the high HF concentration limit. This in part explains the "anhydrous" etching results, since any water present or created by the reaction can be retained in the liquid due to the low H<sub>2</sub>O vapor pressure for high HF concentrations. If the sticking probabilities are equal, that point where the vapor phase and liquid phase partial pressures are equal will be the azeotrope; this occurs at approximately 39 wt.% HF (41), which is near the equal partial pressure points. Therefore, the assumption of equal sticking probabilities is justified. In order to assist in analyzing etching behavior, we have modeled the data used to prepare Fig. 21 using a near regular solution approach, resulting in the curves presented. The model has been refit from our original work (37)-(39) to recent data for the high HF partial pressure limit and all subsequent curves will reflect this fit (114).



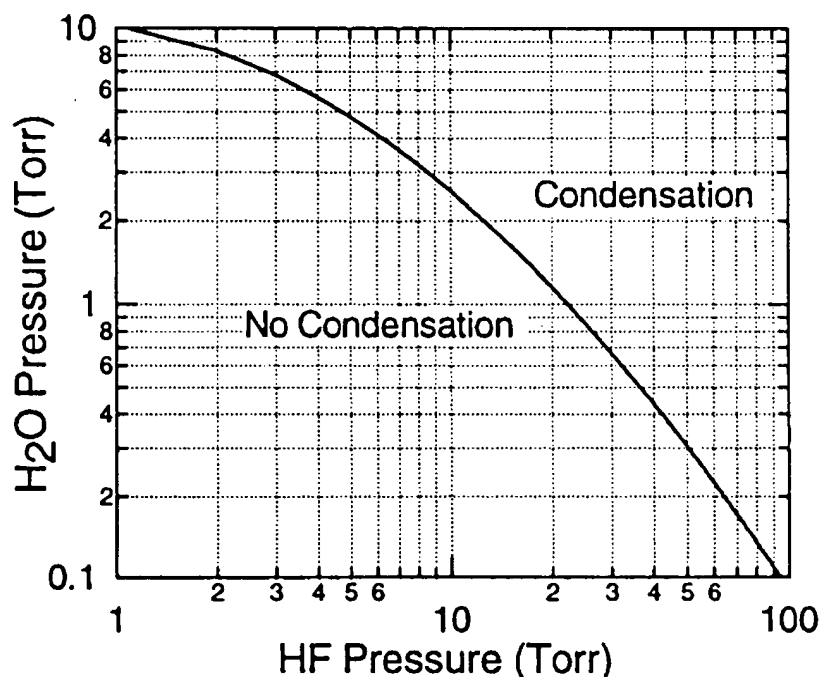
**Figure 21.** Fit to data of Refs. 42 and 114 showing the vapor pressures of both HF and  $\text{H}_2\text{O}$  as a function of HF weight fraction for 20°, 30°, 40°, and 50°C.

At a given temperature a condensed phase will form only if the combination of vapor phase partial pressures is high enough so that the flux of molecules impinging on the surface is greater than that leaving by evaporation. This manifests itself in Eq. (11) where both the numerator and denominator must be greater than zero. This is shown in Fig. 22 for 20°C where condensation will occur on the high pressure side of the line (upper right) and no condensation is expected on the low pressure side of the line (lower left).

So far we have neglected the problem of nucleating a condensed film. For condensation on clean  $\text{SiO}_2$  surfaces this is undoubtedly justified due to the hydrophilic nature of such surfaces. This analysis cannot be applied in other cases and substantially higher pressures for condensation could be required and non-uniformities could also be expected for more hydrophobic surfaces.

**Calculation of Etch Rate.** Having now established the conditions that lead to condensation and therefore etching, we turn our attention to determining the etch rate which can be compared to the liquid etch rates of Fig. 10. This will be affected by the adsorption/desorption process, as well as the consumption of HF during etching and presence of reaction products. For the moment we will ignore these last factors so that we can consider the situation of condensation on an inert surface. Using the data of Fig. 21 via

Eq. (11), the HF concentration as a function of partial pressure can be determined. The etch rate can then be calculated using the value of [HF] and Eq. (6). The predicted etch rate is shown in Fig. 23 at 25°C for various H<sub>2</sub>O partial pressures. Note again the upper left region of this figure corresponds to conditions leading to no condensation and therefore no etching. This also assumes a negligible pressure drop across any boundary layer or pressure gradient due to vapor phase diffusion limitations.



**Figure 22.** Partial pressure diagram indicating what ranges correspond to a stable condensed phase at 20°C.

The comparison of this theory to experiment is difficult since the experimental data reported seldom give values for the reactant partial pressures. Experimental etch rates have ranged from a few Å/sec for conditions where the HF concentration was clearly dilute to hundreds of Å/sec for cases which were reported to be anhydrous (see Figs. 5 and 14). From Fig. 23 we can see qualitatively that these values are in the expected range. In addition, vapor pressure data for the etch results of Deal et al. (59)(60) are available. Fig. 24 shows these experimental vapor phase etch rates as a function of calculated HF concentration in the condensed film. For comparison, the data of Fig. 10 for the liquid case are also shown. The agreement is reasonably good but shows higher vapor phase etch rates at

low concentration and lower vapor phase etch rates at higher concentration. The latter effect may be due to the comparison to liquid rates for stirred conditions as well as the buildup of reaction products. The deviation at low concentration is likely due to the inaccuracy of the vapor pressure model for low HF concentrations where no data were actually available.

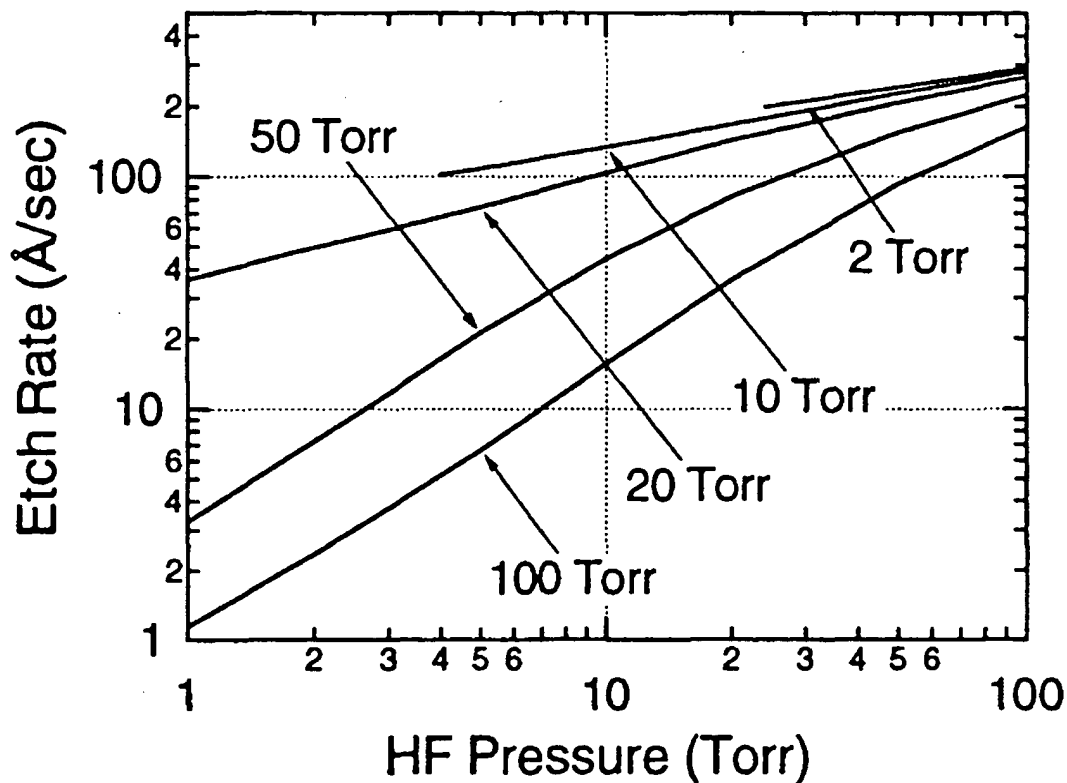
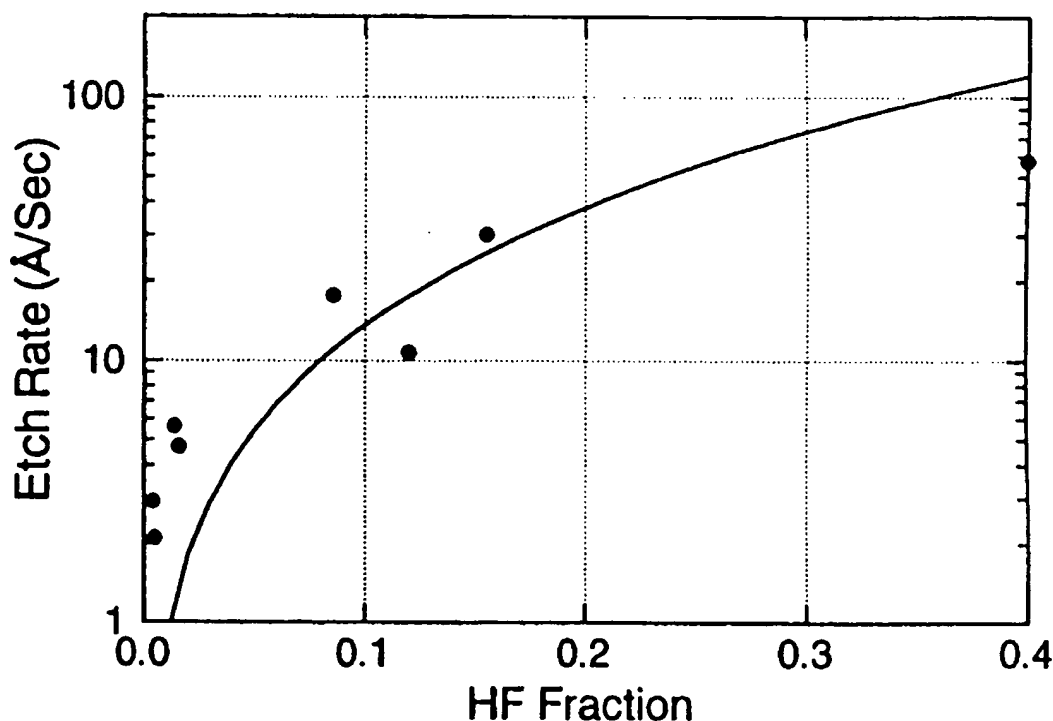


Figure 23. Predicted  $\text{SiO}_2$  etch rates at  $25^\circ\text{C}$  as a function of HF partial pressure for the  $\text{H}_2\text{O}$  pressures indicated, obtained by combining Eqs. (6) and (11).

**Reaction Products and Residues.** The above discussion would correspond reasonably well to the situation early in the etching process where the concentration of reaction products is low. However, as etching proceeds, the reaction products may tend to build up in the condensed layer. If we consider reaction (2), we see six molecules of HF are consumed to form one molecule of  $\text{H}_2\text{SiF}_6$  plus two molecules of  $\text{H}_2\text{O}$ . Therefore the case of "anhydrous" etching would also correspond to a case with a high concentration of reaction products, including  $\text{H}_2\text{O}$ . This points out two disadvantages of vapor phase oxide etching and cleaning: the lack of a nearly infinite source of solvent and the need to remove reaction products by evaporation rather than dissolution. This has been dealt with in some

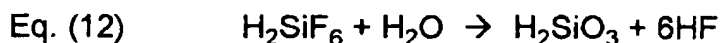


cases with a final water rinse (58), but the addition of a wet step at the end of the process defeats much of the purpose of vapor phase etching and cleaning in the first place. Two vapor phase methods have shown promise for providing residue-free etching and cleaning, one employing HF and H<sub>2</sub>O at elevated temperatures (64)(65) and one employing HF with methanol as the condensable solvent medium (68).



**Figure 24.** Vapor phase etch rates from Refs. 59 and 60 versus equivalent liquid HF fraction calculated from partial pressures using Eq. (11) shown as the points. Actual liquid phase etch rate from Eq. (6) is also shown as the line.

The residues that can form during etching and cleaning occur by the competition between reaction product desorption, represented by Eq. (7), and other reactions which tend to form silicic acids. These can be represented approximately as



The equilibrium suggests that conditions that favor rapid desorption of SiF<sub>4</sub>, high HF pressures, and low water concentrations would lead to less H<sub>2</sub>SiO<sub>3</sub> being formed. Onishi et al. (64)(65) have shown that increasing the reaction temperature by tens of degrees gives much lower residue concentrations.

This is likely related to the greater volatility of  $\text{SiF}_4$  at elevated temperatures (44). Alcohols in place of  $\text{H}_2\text{O}$  as the solvent have also shown improvements in residue formation (68). In this case, reaction (12) is driven to the left by the tendency of  $\text{H}_2\text{O}$  to desorb, leading to lower  $\text{H}_2\text{O}$  concentrations.

There are other implications of the potentially high reaction product limit associated with vapor phase HF etching and cleaning. First, regarding etching itself, Thomsen (43) has shown that  $\text{H}_2\text{SiF}_6$  itself is capable of etching  $\text{SiO}_2$  via



In addition, the presence of high concentrations ( $\geq 10$  mol%) of  $\text{H}_2\text{SiF}_6$  in HF/ $\text{H}_2\text{O}$  solutions significantly reduces the vapor pressures of both HF and  $\text{H}_2\text{O}$  above such solutions. This is an additional mechanism which will stabilize a condensed liquid phase in the high HF concentration "anhydrous" situations, but may also lead to residue formation.

#### 4.4 Summary

From the above discussion it is clear that the etching of  $\text{SiO}_2$  from vapor phase HF/ $\text{H}_2\text{O}$  mixtures occurs after an initiation step by condensation of the HF and  $\text{H}_2\text{O}$ . The subsequent etching occurs by identical mechanisms compared to what would be obtained for liquid phase etching. The major differences between liquid and vapor phase etching are the initiation step, the possible presence of high concentrations of reaction products in the condensed phase, and the need to desorb or rinse off the reaction products after the etch.

Initially it might seem that the "anhydrous" etching results are counter to this model. However, small amounts of water present in the ambient, on the surface, or produced as a consequence of an initial surface reaction, especially in the high HF partial pressure limit are sufficient to produce an HF-rich condensed phase. In addition, the even further reduced  $\text{H}_2\text{O}$  vapor pressure in the presence of high  $\text{H}_2\text{SiF}_6$  concentrations will lead to a condensed phase for "anhydrous" conditions. The model for the low HF concentration limit explains the observed thresholds for etching since, at a temperature which is too high or an HF and/or  $\text{H}_2\text{O}$  pressure which is too low, a condensed phase will not be supported and therefore no etching will occur.

Although we have not specifically discussed mechanisms for the selective etching that has been observed, these effects can be understood qualitatively within the same frame work. The key factor that seems to lead

to differences in selectivity is the water content of the oxide being etched. For low water content oxides or oxide surfaces, higher HF/H<sub>2</sub>O pressures will be necessary to initiate the reaction. This is the case for thermal oxides as discussed above. Native, chemical oxides inherently contain more water so that lower partial pressures will initiate condensation. This effect has been used to provide selective cleaning of native oxides while thermal oxides under the same conditions don't etch at all (58)(60).

### 5.0 IMPURITY REMOVAL

#### 5.1 Types of Contamination

As indicated in the Introduction, several types or classes of contaminants are associated with semiconductor device fabrication. These include particles and residues, heavy metals and ionic impurities, organic and related species, and oxides. These contaminants can come from many sources: equipment, chemicals, ambient, humans, and even the process reactions themselves. A brief summary of analysis and detection methods is presented, followed by a discussion of specific origins and removal methods of impurities using current vapor phase cleaning techniques. These techniques include anhydrous and vapor HF chemistries, vapor HCl and activated Cl<sub>2</sub>, and UV/IR/O<sub>3</sub> combinations. Finally, a short discussion of mechanisms of vapor phase impurity removal will be presented, including an appropriate comparison with aqueous cleaning techniques.

#### 5.2 Evaluation Techniques

A more complete discussion of surface contamination analysis involving device wafers appears elsewhere in this volume (Ch. 12). However, a short summary is appropriate here. Typically, contamination levels which affect device properties have steadily decreased as device feature sizes have shrunk to sub-micrometer dimensions. Thus, critical surface concentrations of impurities, which were originally greater than 10<sup>12</sup> cm<sup>-2</sup>, are now rapidly approaching 10<sup>8</sup> cm<sup>-2</sup>. As often happens, analytical capabilities can barely keep up with detection requirements.

Three general types of analysis procedures are used for surface contaminants. These are so-called "beam" techniques, chemical analyses, and device electrical properties. The latter obviously provide the most sensitive indication of effects of the various levels and types of contami-

nants. The beam techniques include TXRF (total reflection x-ray fluorescence), SIMS (secondary ion mass spectrometry), XPS (x-ray photoelectron spectroscopy), AES (Auger electron spectroscopy), STM (scanning tunneling microscopy), and AFM (atomic force microscopy), among others (115)-(119). In addition, various optical methods, such as ellipsometry and reflectivity, are used to measure thickness of oxide layers and other surface properties (82)(120)(121). These methods range in detection limit from below  $10^{10} \text{ cm}^{-2}$  to 100%, in depth resolution from a few angstroms to 100 Å or more, and in spot size from 100 Å to greater than 1 mm. It is thus obvious that different techniques (or combinations of techniques) will be required for different applications. For instance, SIMS or TXRF would be used for the detection of heavy metals, while Auger or XPS might be used to characterize chemical bonds. Also, correlations of results with electrical characteristics will generally be required for final interpretation.

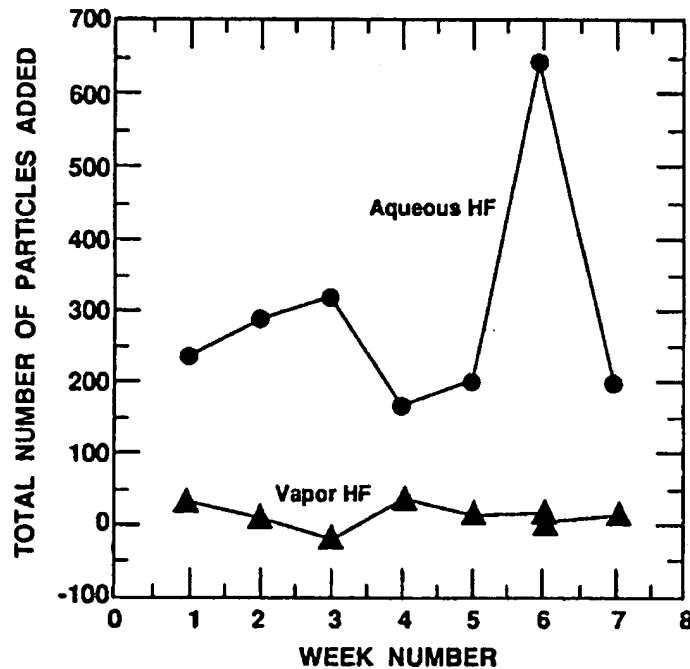
Chemical analyses are being developed either alone or in combination with other methods. For instance, a current method of impurity analysis that shows great promise and appears capable of achieving  $10^8 \text{ cm}^{-2}$  detection levels involves vapor phase decomposition followed by atomic absorption spectroscopy (VPD/AAS) (122). This technique consists of dissolving the native oxide layer in a drop of HF solution which rolls over the surface, pipetting up the HF, and analyzing the drop using atomic absorption. An alternative procedure is to evaporate the drop and use TXRF on the surface. Detection levels of  $10^8 \text{ cm}^{-2}$  have been reported (122) for this method. Other chemical techniques involve rinsing the silicon surface and carrying out appropriate chemical evaluations of the solvent.

Finally, as indicated above, the most sensitive and probably the most relevant analysis technique involves electrical measurements of device related properties. These may be basic properties, such as carrier lifetime, junction I-V characteristics, or surface recombination velocity (123). Or they may involve capacitance-voltage (C-V) analysis, for measurement of ion drift, oxide charges, or charge trapping (124). In addition, such device properties as gate oxide integrity, tunneling oxide endurance, bipolar current gain and speed, and many others can be evaluated as a function of processing variables.

### 5.3 Particles and Residues

One of the critical problems associated with conventional aqueous cleaning of silicon wafers during device fabrication has been that of particles or residue contamination (13)(125)-(127). Particles and residues

can cause severe yield and reliability problems, especially as device feature sizes move to sub-micrometer dimensions. They may be due to the environment, various process equipment, process chemicals and gases, or the actual process cleaning reactions, as well as rinsing and drying. It is now established that many of these problems, especially those involving particles, can be eliminated by the use of vapor cleaning processes. This is especially apparent for HF-last processing where the oxide-free hydrophobic surface is critically sensitive to particles and contamination in aqueous cleaning procedures. Part of this improvement arises because deionized water rinsing, either spray or dip, is no longer needed. A typical example of reduced particle contamination in vapor cleaning compared to aqueous processing is shown in Fig. 25 (66).



**Figure 25.** Particle trends for aqueous and vapor HF native oxide deglaze; after Wong et al. (66). (Reprinted by permission of The Electrochemical Society, Inc.)

The subject of so-called residues is more complex. In the case of oxide etching in HF solutions, for instance, aqueous processes appear to currently have an advantage due to the solubility of typical reaction products and by-products of the reaction in water rinsing solutions. There appear to be two possible solutions to the problem with respect to vapor phase processing. One is the use of a post-vapor etch rinse of some sort. This approach is discussed in (58), and appears to be a satisfactory interim solution to the problem. As integrated processing is developed (see Sec.10), however, a

more basic solution may be required. This will probably involve process chemistry modifications, which may also help to minimize particle contamination as well. For instance, control of pH and composition of the condensed layer on the wafer may provide considerable advantages (64)(65). More than one component or multiple cleaning steps may also be necessary (for instance,  $\text{UV/O}_3 + \text{HF/HCl/H}_2\text{O}$ ).

#### 5.4 Organic Contaminants

For many years, concern about carbon-containing impurities on device wafers has been expressed. However, much of this concern was based on intuitive thinking and speculation, rather than real experimental verification. Even so, various methods were developed for organic impurity removal, most involving UV/ozone chemistry (34)(35). More recently, as vapor phase cleaning technology was being developed, the sensitivity of silicon and oxide surfaces to ambient contaminants, especially hydrocarbons, became much more obvious. One such investigation was especially significant since it demonstrated that common laboratory air and materials could produce considerable organic contamination (88). Furthermore, it was proposed that a good percentage of the so-called "native oxide regrowth" observed using ellipsometric measurement techniques is not due to oxide growth at all, but merely a build-up of these organics and other impurities. (See previous discussions on organic effects on oxide etching in vapor phase systems—Sec. 3.1 and Fig. 12).

The use of UV/ozone chemistries or even heat at lower pressure has proven successful in removing unwanted organic impurities from wafer surfaces. Investigations involving these types of pre-cleaning treatments have been carried out in molecular beam epitaxy investigations, or even by conventional low temperature epitaxial processing (128)-(130). Some of these investigations have involved activated "dry" processes, but as was noted earlier, radiation-producing reactions such as plasma and sputtering tend to cause undesirable effects on device properties.

While millions, and probably billions, of dollars have been spent on minimizing particles in wafer fabrication environments, very little effort or cost has been expended in removing chemical impurities. Therefore, it is expected that either considerable attention must be paid to this particular problem, or new types of wafer fab facilities must be developed. Extensive filtering systems or integrated processing technology (discussed in Sec. 7.0) may be the answer.

### 5.5 Metallic Contaminants

It has long been known that heavy metal impurities can result in severe yield and reliability problems in silicon devices. These impurities are typically Fe, Cu, Zn, Ni, Cr, and even Au. They can originate at any process step, even with the starting silicon material. They will affect a variety of device characteristics, including junction leakage, surface and bulk recombination, emitter to collector shorting, and even gate oxide integrity. In addition to heavy metals, light elements such as C, Al, S, and even the alkali metals (Na, K, Li) can result in catastrophic failures in devices.

It is essential that all metallic impurities be analyzed and controlled to suitable minimum concentrations. This control may be difficult and depends on the location of the metal species in or on the device wafer, as well as its chemical nature. For instance, it may be located on top of an oxide layer, within the oxide, at the oxide-silicon interface, or even in the silicon itself. It also may be in elemental form, or as a compound such as an oxide or carbide. Thus, these properties of the metal impurities can determine the nature of the optimum removal process itself, whether it be gettering, aqueous cleaning or vapor type cleaning. It is possible that combinations of these may be appropriate.

Of all the types of impurities discussed above, vapor phase removal of metallic impurities has proven the most difficult. Part of this difficulty has been due to the high temperatures required for vaporization of metallic compounds such as oxides or halides. Also, the location of the metal impurities has posed some problems. On the other hand, aqueous cleaning followed by a water rinse has proven more satisfactory since most of the metal compounds are water soluble and can be rinsed away. Even so, it is believed that overall possibilities for vapor phase metal removal remain good, especially when considering related particle and organic impurity cleaning processes. A more detailed discussion on mechanisms and future possibilities involving vapor cleaning techniques follows.

Some investigations are now being reported concerning vapor phase removal of metallic impurities from silicon wafers. These involve HF chemistries (55)(59), combinations of HF and UV/ozone (131), dry HF-H<sub>2</sub>O combinations (58), other gas chemistries (132), and UV excited Cl<sub>2</sub> processes (54). Data showing the effectiveness of HF/H<sub>2</sub>O cleaning for metal impurity removal from silicon surfaces, with and without a post-clean DI water rinse, are shown in Fig. 26 (58). In the UV/Cl<sub>2</sub> case, photoexcited chlorine species are used to etch a thin silicon layer, thus removing metal impurities incorporated on or in the silicon. Mechanism of metal removal

may be by volatilization of the metal halide or by liftoff. A critical part of this process involves the uniformity and control of etching the silicon layer. Data demonstrating this silicon etching are shown in Fig. 27, as reported by Ito (133).

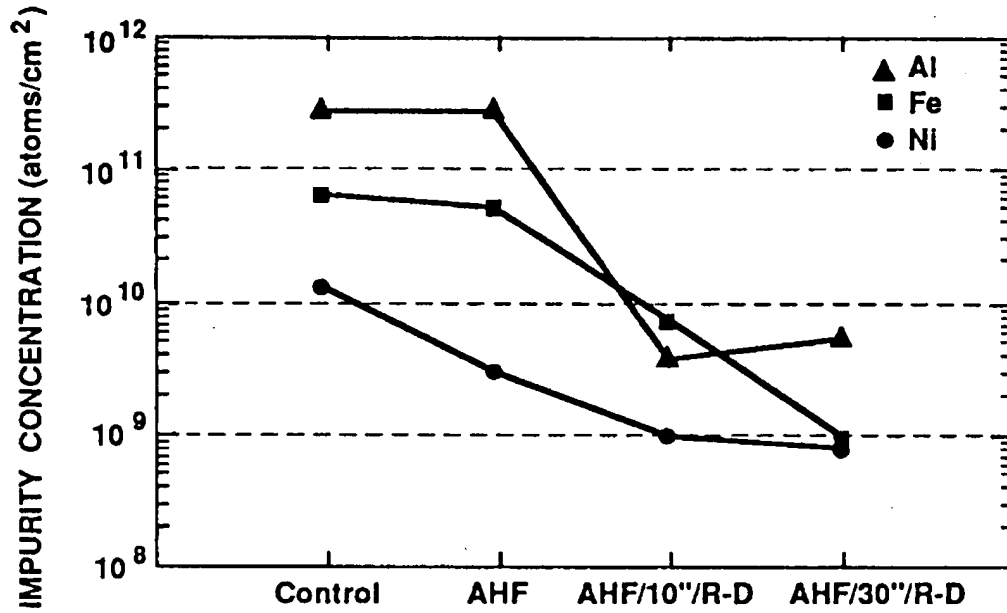


Figure 26. Metallic impurity removal by integrated etch rinse processing; after Syverson (58).

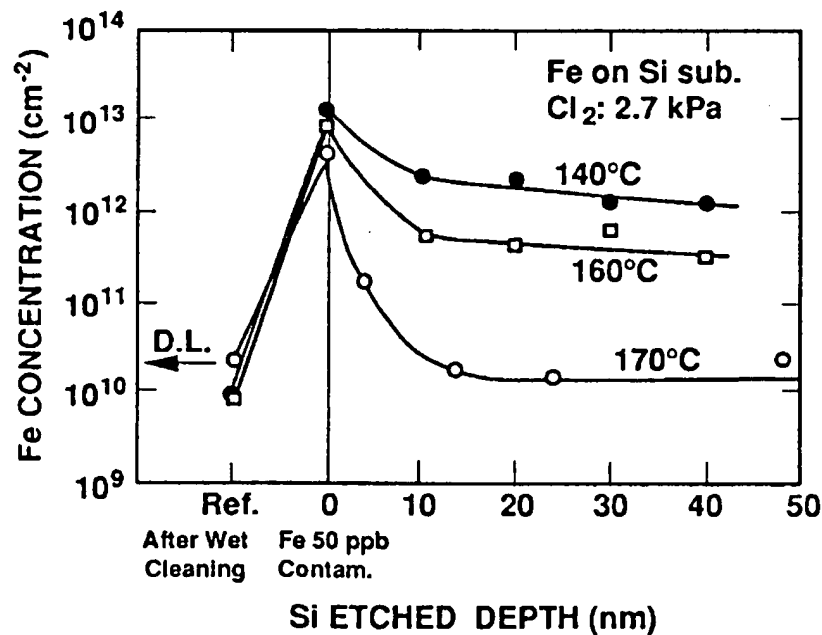


Figure 27. Iron concentration on the silicon surface before and after UV-excited dry cleaning; after Ito (133).



## 5.6 Mechanisms of Metal Impurity Removal

Vapor phase metal removal requires that the metal be in a form that can be volatilized, which typically requires elevated temperatures as well as the formation of a more volatile compound. For the purposes of this discussion we will assume that temperatures above 400°C are unacceptable for typical cleaning processes. Even at this temperature, however some metals may be volatile enough so that they can simply be thermally desorbed. This is illustrated in Fig. 28 where the vapor pressures of volatile metals are plotted versus temperature from the tabulations of Kubaschewski and Alcock (134). The right axis is the equivalent flux, assuming the sticking probabilities are unity for equilibrium vaporization. A vapor pressure of  $10^{-6}$  torr corresponds to a equivalent flux of approximately one monolayer/sec, sufficient for removal of the metal in reasonable times. From this curve, therefore, we might expect all these metals to be volatile enough for simple thermal cycling to be sufficient to remove them. However, the analysis assumes that the metals are not chemically bonded to Si, oxygen, or other species. This may not be the case for Li, Ca, Mg, and Sr, which form both stable oxides as well as silicides. Na and K oxides are not stable in contact with Si, but with stable silicides this approach may not be effective with them either. Of the volatile metals, Zn, Cd, and Pb have the best chance for this process to work, since they don't have stable silicides and their oxides are unstable with respect to Si. We note at this point that this analysis (and that to follow) is rather speculative, and we know of no experimental data to test these ideas at this time.

A method that has been examined experimentally is the use of chlorine (normally excited by UV radiation) to produce volatile species of the metals which can be desorbed. A plot for some metal chlorides similar to that of Fig. 28 for the pure metals is shown in Fig. 29. The experimental results obtained on many of these metals can therefore be understood based on simple evaporation of volatile chlorides. However, Ito (133) has observed significant cleaning efficiencies at 170°C, below what would be necessary for this mechanism alone (except for possibly Fe). It seems likely that the UV radiation or the joint evaporation of  $\text{SiCl}_x$  may well catalyze the metal chloride removal; it is also possible that some volatile metal-Si-Cl complex may form as well.

A difficulty with this method appears to be related to the rapid reaction and desorption rate of Si in the form of  $\text{SiCl}_2$  or  $\text{SiCl}_4$  under conditions that lead to efficient metal removal. The tendency for this to occur is also illustrated in Fig. 29 where the  $\text{SiCl}_2$  and  $\text{SiCl}_4$  vapor pressures are shown. Methods to retard this Si etching and the surface roughness it can cause are an active area of research today.

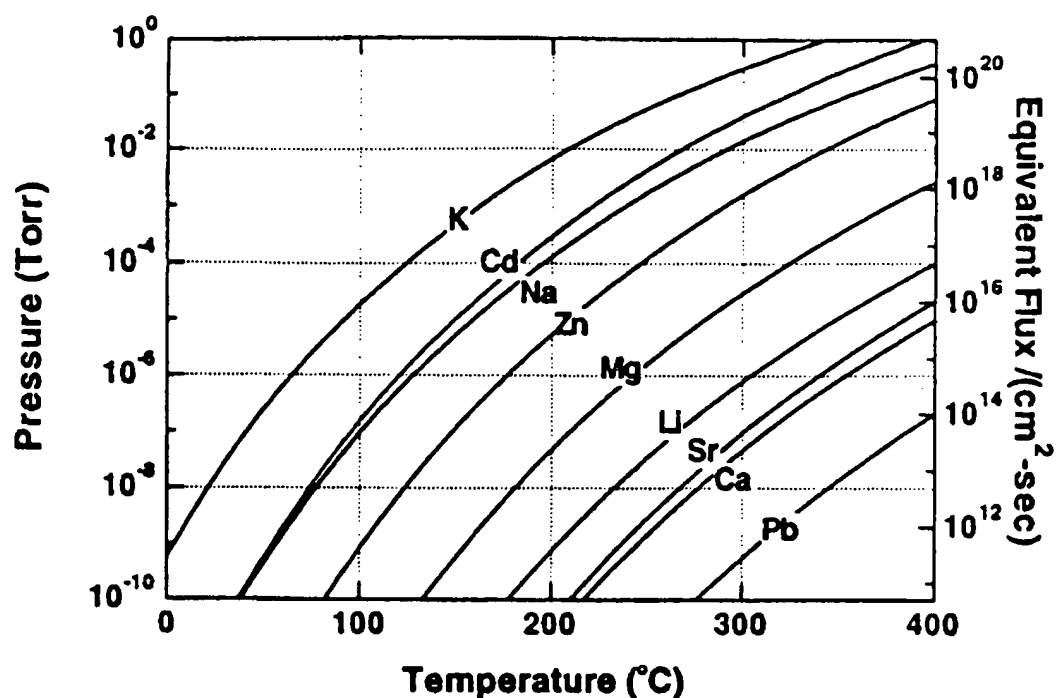


Figure 28. Vapor pressures for "high" vapor pressure metals as a function of temperature; the right hand axis would correspond to the equivalent flux leaving the surface assuming a unity equilibrium sticking coefficient and molecular flow.

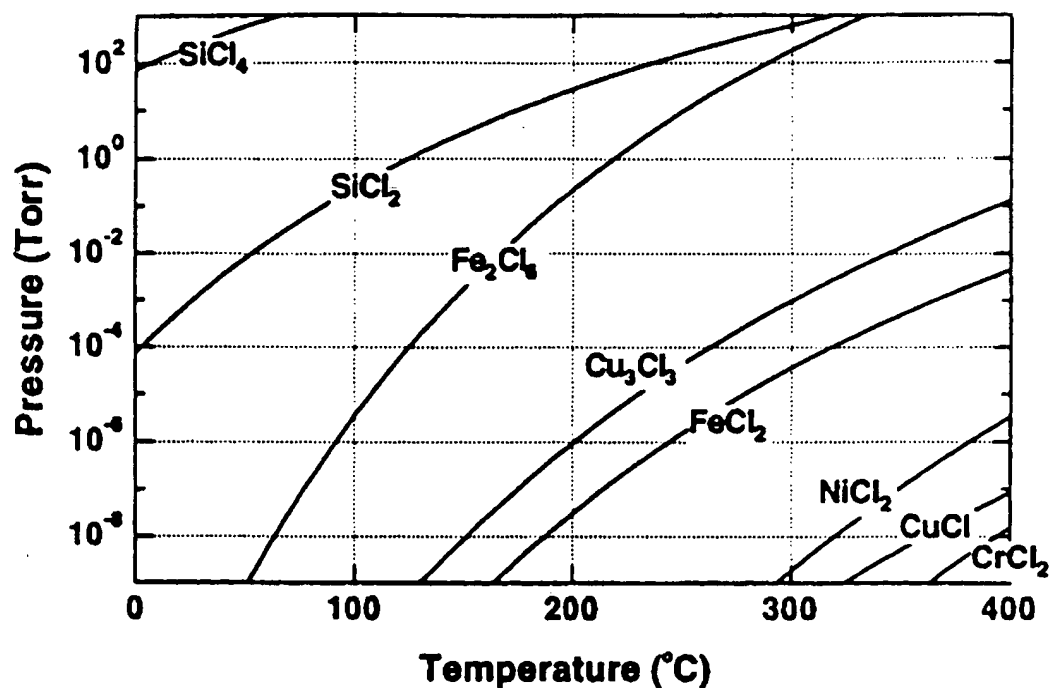


Figure 29. Vapor pressures for some important metal chlorides showing their volatility at temperatures used in UV enhanced vapor phase metal cleaning.

## **6.0 DEVICE APPLICATIONS**

### **6.1 General Effects of Impurities on Device Properties**

The fact that impurities can adversely affect both yield and reliability of semiconductor devices has been known from the days of the first silicon devices. Even though tolerance to impurity concentrations was much greater in the late 1950s, considerably higher levels of contaminants were also present. Over the years, as manufacturing and process procedures improved and contamination levels decreased, so did device feature sizes, and device purity requirements correspondingly increased. Thus the process engineer has continually been on the edge of his or her ability to maintain an impurity level low enough to achieve satisfactory device performance.

As was indicated above, several types of impurities must be controlled. Effects of characteristics generally fall into three main categories. These are: (1) junction characteristics, (2) contact or interface properties, and (3) MOS gate oxide properties. There are obviously some overlaps, such as MOS gate oxide - semiconductor interfaces. General considerations and application examples regarding these three categories are presented below with respect to vapor phase cleaning.

### **6.2 Junction Characteristics**

A reasonable number of papers have been published relating impurity effects to junction characteristics (135)(136) but most of these deal with liquid precleans or gettering for the removal of contaminants from the junction region. It is anticipated that vapor cleaning technology will be successful in minimizing contaminant effects on junctions, but for now not much information is available.

### **6.3 Contact/Interface Properties**

A number of device structures involve contacts or interfaces of some kind. These include: (i) metal-silicon or metal-metal contacts, (ii) epitaxial silicon-substrate silicon interfaces, (iii) poly-silicon-substrate silicon interfaces, and (iv) oxide- or dielectric-substrate silicon interface. Some of these, (i) and (ii), require a minimum of resistance and thus as thin an oxide interface layer as possible. On the other hand, (iii) can involve poly-Si bipolar emitter structures and for this application, a thin, uniform oxide

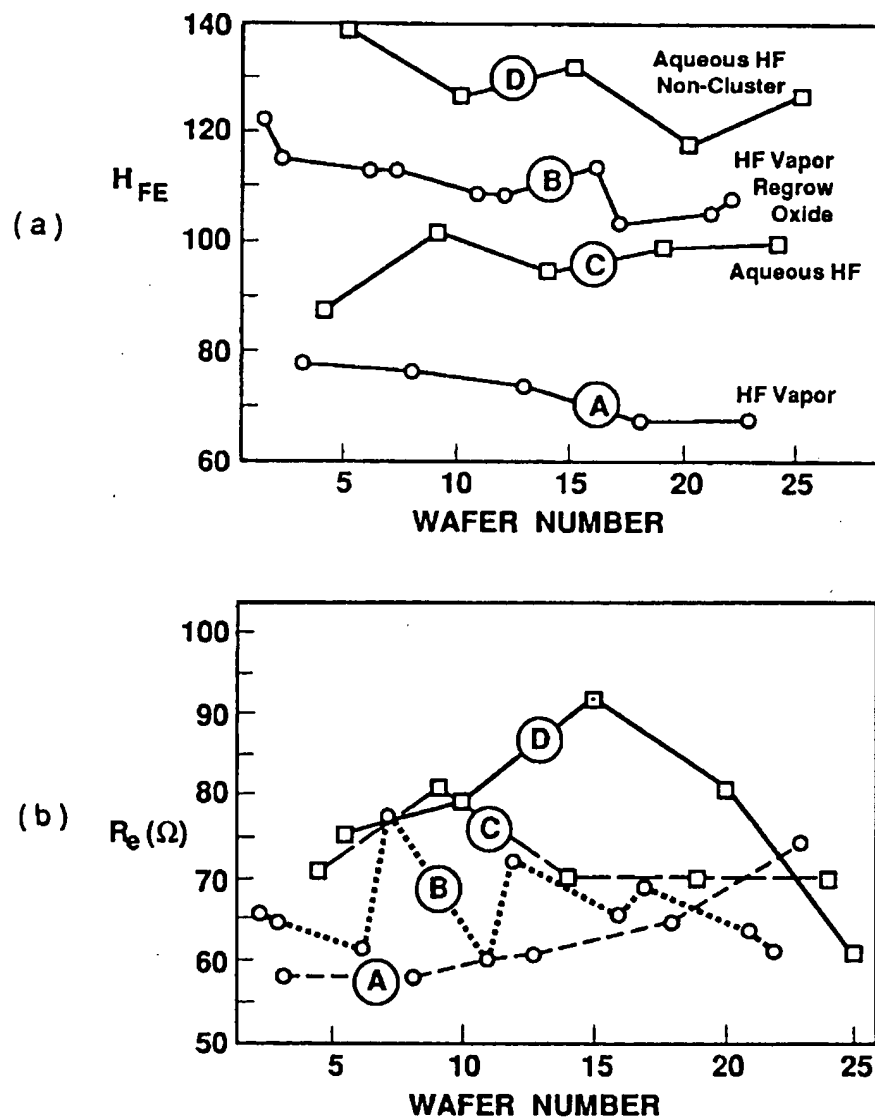
(about 10 Å) is often preferred. In the case of (iv), the resistance is not a factor, but rather minimum structural defects which lead to interface traps are desired for optimum device performance. In all cases, proper cleaning of the surface prior to film deposition or oxide formation is necessary to remove all unwanted impurities including native or chemical oxides.

Various results have substantiated that vapor phase cleaning can result in improved surface and interface characteristics. Often this requires only vapor hydrofluoric acid (57). In the case of pre-epi-Si cleaning, several examples have been reported which demonstrate the effectiveness of vapor HF pre-clean (137)(138). Because a final water rinse is often not necessary, less oxygen, as well as carbon and other impurities, are found after vapor cleaning at the epi-silicon interface. The same is true for various structures involving metal contact depositions on silicon. Along related lines, it has been determined that the presence of any water on a doped polysilicon surface will prevent satisfactory adherence of metal silicide films. The use of vapor phase HF cleaning prior to silicide deposition completely eliminates this problem. Yield data tabulated in Table 3 demonstrate the effectiveness of a vapor phase HF pre-clean for tungsten silicide adherence.

**Table 3. Effect of Pre-Clean Process on Tungsten Silicide Lifting**

■ VAPOR PHASE HF CLEAN		
WAFER NO.	SILICIDE LIFTING / DELAMINATION	
	NO. LIFTED AREAS	NO. DIE INSPECTED
1	1	33
3	0	33
5	1	33
7	1	33
9	0	33
11	0	33
TOTALS	3	198
PERCENT FAILED	1.5	
■ STANDARD AQUEOUS CLEAN		
WAFER NO.	SILICIDE LIFTING / DELAMINATION	
	NO. LIFTED AREAS	NO. DIE INSPECTED
2	3	33
4	21	33
6	12	33
8	16	33
10	6	33
12	26	33
TOTALS	84	198
PERCENT FAILED	42	

In the case of poly-Si emitters, more uniform, better controlled device characteristics have been obtained for vapor HF precleans (139). Figure 30 indicates results obtained where vapor HF was compared with other types of cleans, with and without integrated in situ processing. The results demonstrate that optimum results will require a thin, controlled oxide film to optimize both current gain and contact resistance. Finally, the interface between a gate oxide and the substrate must be properly cleaned to remove metals, ionics, carbon, and other impurities which contribute to the formation of interface charges (124)(140).



**Figure 30.** (a) Effect of various HF pre-treatments on current gain ( $H_{FE}$ ) of poly-Si emitter transistors. (b) Effect on emitter resistance ( $R_e$ ); after deBoer and van der Linden (139). (Reprinted by permission of The Electrochemical Society, Inc.)

## 6.4 Gate Oxide Properties

Integrity of the thin gate oxide is perhaps the most critical property of MOS devices, and it is the most dependent on contaminants such as heavy metals or particles. These contaminants are generally present on or in the silicon prior to gate oxidation and become incorporated in the oxide as it is formed. The oxide integrity normally is reflected by low dielectric breakdown or even direct electrical shorts. Various tests are employed to evaluate gate oxide integrity. These include ramped voltage or field breakdown ( $V_{BD}$  or  $E_{BD}$ ), charge-to-breakdown ( $Q_{BD}$ ) or time-dependent dielectric breakdown (TDDB). Comparisons of vapor phase versus conventional liquid gate oxidation pre-cleans are now being reported which indicate improved oxide integrity for vapor HF pre-cleans (66)(67)(141). It is believed that vapor processes result in a reduction of particles and other impurities on the surface which helps to account for this improvement. A typical comparison of TDDB obtained for vapor and liquid pre-cleans is presented in Fig. 31.

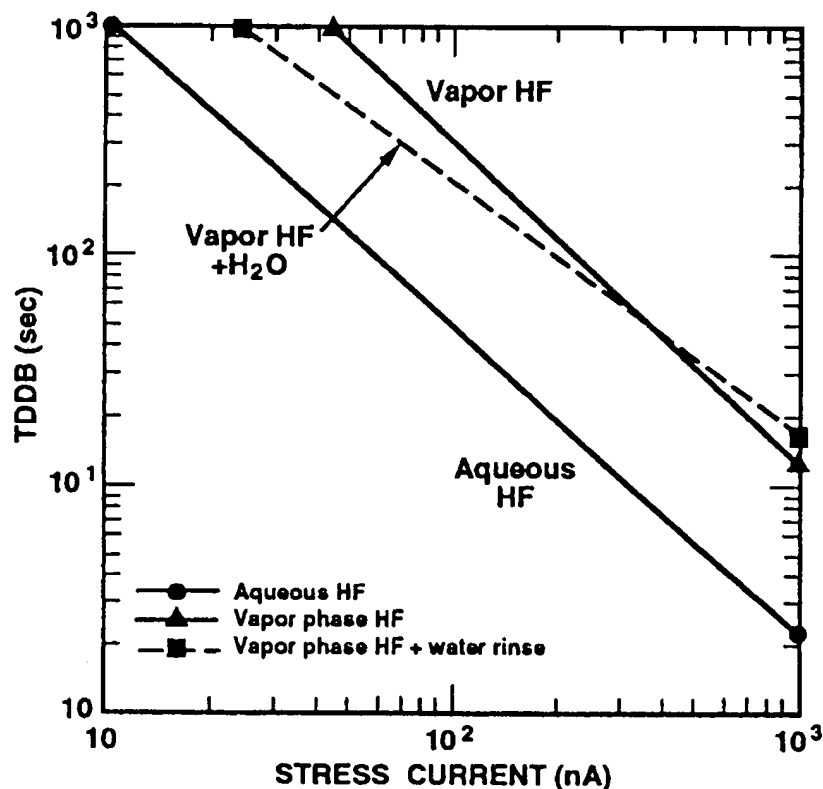


Figure 31. Effect of gate oxidation pre-clean on TDDB (time-dependent dielectric breakdown) using constant current stress; after Wong et al. (66). (Reprinted by permission of The Electrochemical Society, Inc.)

It has recently been noted (108)-(110) that silicon surface roughness is also partially responsible for low dielectric breakdown in gate oxides. This is undoubtedly due to higher electric fields at non-uniform areas of the oxide, which are caused by the rough silicon surface during oxidation. However, contaminants undoubtedly contribute as well. A primary cause for rough silicon has been found to be due to etching of the silicon by the ammonium peroxide liquid clean treatment. The effect is reduced by decreasing the ammonium hydroxide concentration. Typical results are shown in Fig. 32. The roughness effect is not observed after vapor phase cleaning treatments, unless they follow directly the liquid ammonium peroxide step.

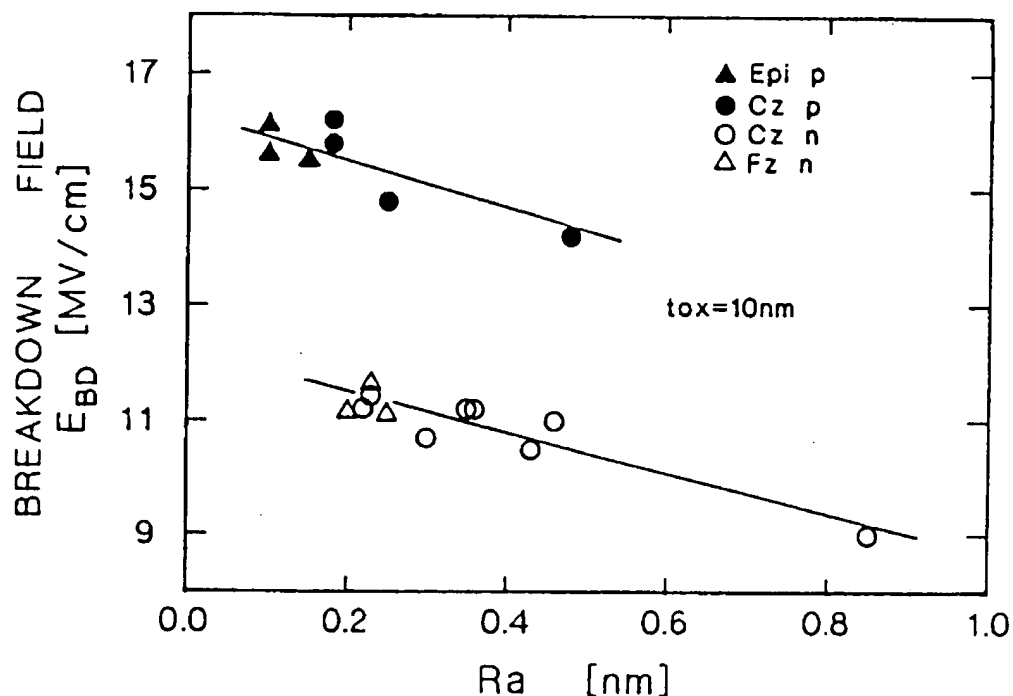


Figure 32. Surface microroughness dependence of gate oxide breakdown field; after Ohmi (109).

Another problem observed with gate oxides caused by surface contamination is excess carrier trapping in the oxide. This is especially critical with respect to memory-type devices where so-called "tunneling oxides" are employed. It is also important for devices exposed to ionizing radiation. The latter involves the same effects mentioned earlier where radiation-produced defects result from "dry" cleaning processes. Not only have vapor cleaning processes been found to incorporate fewer impurities in the

oxides which can lead to charge or carrier trapping, but fluorine species left on the surface after vapor HF cleaning appear to provide trap- or radiation-resistant oxides (142)-(144). Somehow, the fluorine species neutralize the oxide traps and significantly retard charge trapping.

One other effect of contamination on gate oxide technology is that of oxidation kinetics. It has been determined that a preoxidation clean involving ammonium peroxide ( $\text{NH}_4\text{OH} + \text{H}_2\text{O}_2$ ) can retard the rate of oxidation (145). Later investigations (146)-(148) indicated that this retardation was due to aluminum impurities in the cleaning solution, probably from the hydrogen peroxide. In addition, for very thin oxides ( $< 100 \text{ \AA}$ ) the effect is reversed, and the oxidation rate is faster for aluminum-contaminated ammonium peroxide treatments. A kinetic plot is shown in Fig. 33 which demonstrates the effect of  $\text{NH}_4\text{OH} + \text{H}_2\text{O}_2$  versus HF pre-oxidation cleaning treatment. The solution to the problem obviously involves the use of higher purity chemicals.

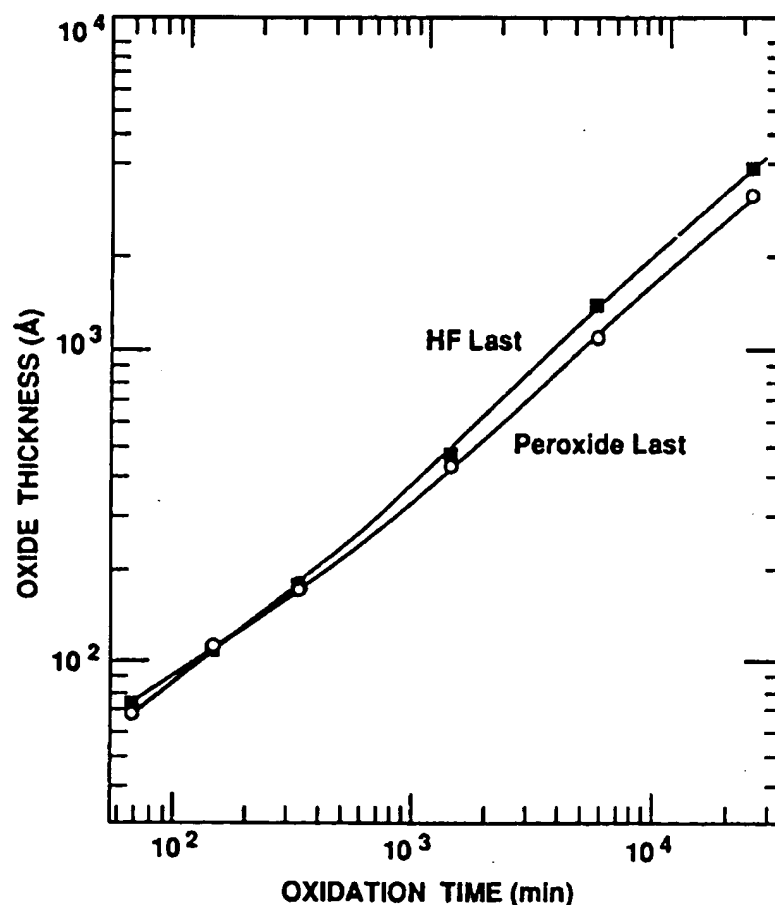


Figure 33. Best fit of present oxidation model to reverse-RCA and HF-cleaned surfaces for 800°C dry  $\text{O}_2$  oxidation of (100) silicon; after deLarios (148).



## 7.0 INTEGRATED PROCESSING

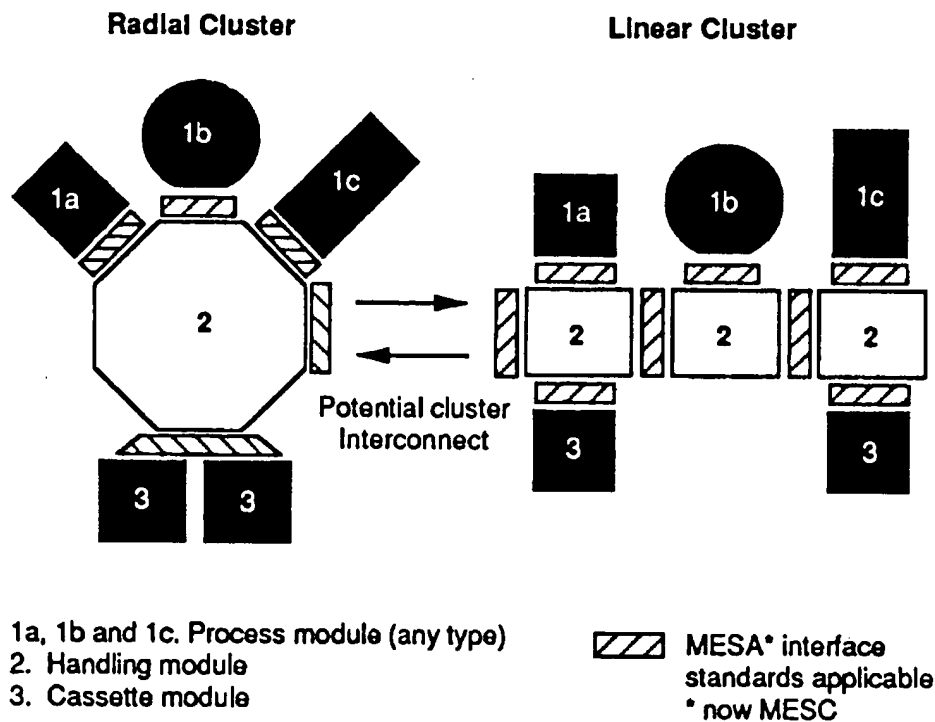
### 7.1 Concept

Integrated processing is the term or expression normally used to describe the combination of two or more sequential processes in semiconductor device fabrication whereby these processes are carried out in situ in a controlled ambient. Often such processes involve a film deposition onto a silicon surface, and the resulting interface is critically dependent on the cleanliness of that surface. A typical example might involve a silicon cleaning treatment followed by the deposition of a contact metal such as aluminum. A more complex sequence would be the preparation of a MOS gate structure, where the integrated processing sequence would involve (i) sacrificial oxide strip, (ii) gate oxide pre-clean, (iii) gate oxidation, and (iv) poly-Si gate deposition. Thus the cleanliness of two critical interfaces ( $\text{SiO}_2\text{-Si}$  and poly-Si- $\text{SiO}_2$ ) is preserved by controlling the ambient and surface cleanliness throughout the multi-process sequence.

The cluster-tool configuration, used to carry out integrated processing, typically consists of a central automated handling system which transports device wafers from a loading station to and from various process modules. When the process is complete, the wafers are transported to an unloading station. The wafers are exposed during transport (and in the handler) to only vacuum or an inert gas such as argon or nitrogen. Vacuum level is usually maintained at least to  $10^{-5}$  torr. While concepts for cluster tools are still developing, configurations are generally radial or linear. Schematic examples of these two types are shown in Fig. 34.

Several reviews which discuss the current status and future potential of integrated processing and cluster tool concepts are available (150)-(160). Certain conclusions may be drawn at the present time. First, it is apparent that only vapor or gas type processes will be practical in such systems. Thus, conventional liquid-type wafer cleaning processes will not be acceptable, providing considerable support for the concept of vapor or gas phase cleaning technology. Also, single wafer processing will be required which will impact such factors as throughput. This will be discussed below. Finally, it is not clear at this time how far the idea of integrated device processing can be taken. In other words, How soon, if ever, will the technology allow the often-spoken "sand-to-device-in-a-box" concept? It is much more likely that small numbers of processes (two to five) will be combined into small cluster groups, and wafers will be transferred from one group to the next by some appropriate method such as SMIF (161)(162). In any case, it is anticipated that the days of mega-dollar clean rooms may be numbered.

### Modular System Concepts



**Figure 34.** Schematic of radial and linear cluster configurations for integrated processing; after Van Leeuwen (149).

## 7.2 Advantages and Disadvantages of Integrated Processing

Several of the reasons for developing integrated or cluster tool processing for sub-micrometer device fabrication have already been given above, but a short summary of potential advantages and disadvantages (challenges) is appropriate. First, and probably most important, is the fact that tomorrow's device structures probably cannot be produced without reducing contamination levels several orders of magnitude from today's capabilities. This can only be accomplished by better controlling the ambient to which wafers are exposed during fabrication. Along these same lines, integrated processing, even on a limited basis, will allow more efficient and flexible processing. It should also result in fewer process steps as well, with much greater process control through computerized monitoring and programming of the process sequences. Finally, greater cooperation and planning between equipment manufacturers and device engineers will be required which will undoubtedly lead to improved overall results.

Integrated processing will also lead to additional challenges. It should be expected that any new complex equipment, as these systems are, will pose reliability questions which must be resolved. Since this technology utilizes single wafer processing, then thruput will be a consideration. Another challenge in this type of concept will be the matter of compatibility, both from a standpoint of module alignment and space considerations, but also questions of interference among the various reaction gases and ambients. For instance, one process may operate at semi-high vacuum and can't tolerate water vapor, while the next module may involve a water-saturated cleaning treatment. Finally, Is vapor-phase, integrated processing adaptable to all types of processes required for device fabrication? What about lithography? All of the questions and challenges must be considered and satisfactorily solved.

### **7.3 Requirements/Considerations of Integrated Processing**

In addition to the discussion above related to advantages and challenges of integrated wafer processing, it is worthwhile to summarize the main requirements and other considerations of this technology with emphasis on wafer cleaning. First, the requirement for vapor cleaning processes in integrated processing has already been emphasized. In addition, the single wafer concept is already well established in vapor cleaning technology, and is rapidly becoming common in other processes. The same is true for the use of computer-controlled, automated systems of all types.

An area that at present is somewhat lacking in vapor cleaning systems and will be very important in cluster tools is that of in situ monitoring and control. It will be very desirable, for instance, to be able to measure oxide thickness as it is being etched back in HF/H<sub>2</sub>O chemistries. Similarly, determining complete removal of an oxide to a hydrophobic surface would be most important. Monitoring particle concentration on the wafer, as well as in the ambient in situ, will provide a lot better control of the process. Of course, temperature and pressure monitoring are already being accomplished in the currently available cleaning systems. Likewise, gas reactant composition is being monitored and controlled by a wide variety of RGAs (residual gas analyzer). The ultimate, however, will be to have the capability to measure surface impurity levels as the wafers are being cleaned. This will require analytical beam techniques, such as TXRF (total reflection x-ray fluorescence spectroscopy), to be incorporated in the reaction module (116). Hopefully most of these capabilities will be possible in the not-too-distant future.

#### 7.4 Applications Involving Vapor Cleaning

Investigations are already being reported on the use of integrated processing for selected critical sequences in device fabrication. Even though these tend to be limited to a few steps, they show the great potential for this kind of technology. As might be expected, all of them include a pre-process cleaning step, and this cleaning involves vapor or dry processing. Following is a summary of reported results.

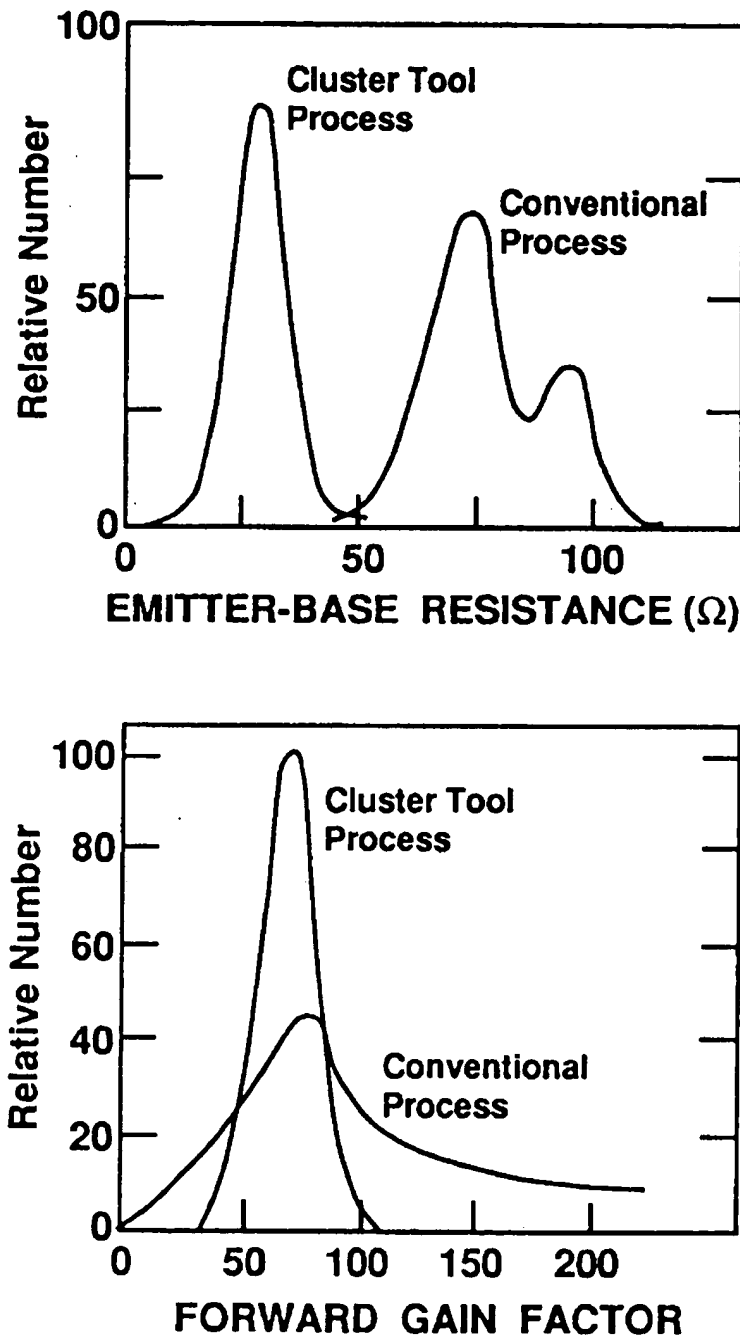
**MOS Structure.** This process sequence includes gate oxide pre-clean (may include sacrificial oxide strip), gate oxidation, and finally poly-Si gate deposition. As indicated earlier, this sequence includes two of the most sensitive interfaces from the standpoint of contamination effects. Results reported involving part or all of the above sequence indicate significant improvements in gate oxide quality of MOS structures (163)-(166).

**Metal or Poly-Si Contacts.** Another natural application for vapor cleaning/integrated processing involves metal or poly-Si contacts to silicon. This can be accomplished rather simply by combining a pre-clean with the metal deposition. As is the case for MOS structures above, initial reported results appear very promising.

**Epitaxial Silicon Deposition.** It was mentioned above that epitaxial silicon deposition following a pre-clean involving gaseous HCl represents the first example of integrated processing (18). Also, MBE (molecular beam epitaxy) scientists have used various vapor or gas type precleans for the preparation of exotic structures—both silicon and compound semiconductor-based (137). More recently, investigators have demonstrated the use of in situ vapor cleaning processes in combination with lower temperature (750°C or thereabouts) silicon epitaxial deposition (137)(138). The results indicate that such integrated processing will be required for contamination-free epi deposits, especially as process temperatures drop even further.

**Bipolar Poly-Si Emitter Structures.** The poly-Si emitter structure in bipolar device technology has shown great promise but has been very difficult to prepare. In this technology, the poly-Si is deposited onto a single crystal region. An n-type dopant, such as arsenic, implanted into the poly-Si is diffused into a shallow, p-type base region to form the emitter. The presence of (or lack of) a thin oxide layer between the poly-Si and single crystal silicon regions will affect both current gain and emitter resistance. Results now demonstrate that integrated processing permits in situ removal of the initial thin oxide by vapor HF, regrowing a controlled 10 Å oxide, and then depositing the poly-Si. The resulting bipolar device exhibits tighter distribution of both emitter resistance and current gain (139)(167). Results

have been plotted in Fig. 35. Thus, device characteristics can be tailored by controlling the thickness of the regrown oxide interface layer. Other similar results have been reported (168)(169).



**Figure 35.** Distribution of emitter-base resistance and gain comparison between cluster tool process and conventional process; after Werkhoven et al. (167).

**Sidewall or Trench Passivation.** One other application of vapor cleaning combined with integrated processing involves the passivation of sidewall or trench structures. In this situation, polymeric and other residues remaining from reactive ion etching are removed from the sidewalls by vapor cleaning, which is followed by suitable thermal oxidation or CVD deposition of various dielectric films. As with the other examples described above, improved results are obtained by this combination (109)(110).

## 8.0 CONCLUSIONS AND SUMMARY

In this chapter, we have reviewed vapor phase wafer cleaning technology. After summarizing historical developments and practices concerning silicon wafer cleaning which primarily involved aqueous technology, the concept of vapor phase wafer cleaning technology has been presented and discussed in detail. This discussion includes historical trends which justify the incorporation of vapor cleaning processes in current or future advanced device fabrication facilities. One of these justifications is the requirement for the cleaning reagent to penetrate deep trenches or grooves in the  $0.5\ \mu\text{m}$  range or below. Another is the critical requirement to simplify process and facility complexity and cost. Still another relates to environmental concerns. It should be recognized, however, that as of this date (1992), vapor phase cleaning only exists in current production lines on a very limited basis. On the other hand, it is evident that this concept is overwhelmingly endorsed by most engineers looking toward the future.

One of the important aspects of current and future device fabrication involves the uniform removal or etching of oxide layers. Examples have been presented showing how such etching can be carried out, both in blanket form across a wafer as well as in selected regions. The concept of "native oxide" formation and regrowth has been reviewed. In addition, we have discussed differences in etch rates and reaction mechanisms for different types of oxides and dielectric films. Moreover, a detailed discussion of mechanisms involved in vapor phase etching, and cleaning in general, has been presented, which should help considerably in the development of more advanced cleaning processes in the future.

Finally, we have discussed the importance and requirements for reducing the levels of various types of contaminants using vapor phase cleaning. These impurity types include organics, oxides, particles and residues of all kinds, and different kinds of metals. It is believed that the difficulty of accomplishing such minimization of these contaminants by

vapor cleaning increases in the order listed above. In other words, a form of vapor cleaning, ultraviolet light plus ozone, has been used for some time to remove exposed resist from wafer surfaces. On the other hand, at least some of the metals may be very difficult to remove completely using known vapor cleaning techniques without subsequent water rinsing.

We strongly believe, however, that for device complexities and feature sizes of the future (1 Gbit and 0.2  $\mu\text{m}$ ), vapor cleaning will be an absolute requirement. Many engineers also feel that an HF-last process with no subsequent rinse will provide the most optimum surface for enhanced device performance and reliability. This will best be accomplished using vapor technology. It is also believed that some form of integrated, in situ processing involving so-called "cluster tools" will solve many of the current technical, financial, and environmental problems that seriously limit future advances in integrated circuit technology.

#### ACKNOWLEDGMENTS

The authors wish to thank T. Ohmi of Tohoku University, Sendai, Japan, for providing Figs. 14 and 30, D. B. Deal, M. Kohl, and D. Syverson of FSI International for providing Figs. 4, 5, 16, and 25, and G. Higashi of AT&T Bell Laboratories for providing Fig. 20. Helpful discussions with J. M. deLarios, D. B. Kao, M. A. McNeilly, and G. L. Nobinger of Advantage Production Technology, and M. Wong and M. Moslehi of Texas Instruments are gratefully acknowledged. One of us (CRH) would also like to acknowledge financial support from Advantage Production Technology, Texas Instruments, SEMATECH through Advantage, and Stanford's Center for Integrated Systems.

#### REFERENCES

1. *Symposium on Cleaning of Electronic Device Components and Material*, 246, ASTM, Philadelphia (1958)
2. Faust, J. W., Jr., in: *Symposium on Cleaning of Electronic Device Components and Materials*, 246:66, ASTM, Philadelphia (1958)
3. Khilnani, A., in: *Particles on Surfaces I, Detection, Adhesion, and Removal*, (Mittal, ed.) p. 17, Plenum Press, Thornwood (1986)
4. Kern, W. and Puotinen, D. A., *RCA Review* 31(6):187 (1970)

5. Kern, W., *RCA Engineer* 28(4):99 (1983)
6. Kern, W., *J. Electrochem. Soc.* 137:1887 (1990)
7. Kern, W., *Semiconductor International* 7(4):94 (1984)
8. Amick, J. A., *Solid State Technology*, 19(11):47 (1976)
9. Henderson, R. C., *J. Electrochem. Soc.* 119:772 (1972)
10. Tolliver, D., *Solid State Technology*, 18(11):33 (1975)
11. Burggraaf, P., *Semiconductor International*, 13(7):58 (1990)
12. Burkman, D., *Semiconductor International*, 4(7):103 (1981)
13. Walter, A. E. and McConnell, C. F., *Microcontamination*, 8(1):35 (1990)
14. Jurcik, B. J. Jr., Brock, J. R. and Tractenberg, I., *J. Electrochem. Soc.* 138:2141 (1991)
15. Schwartzman, S., Mayer, A. and Kern, W., *RCA Review*, 46(3):81 (1985)
16. Skidmore, K., *Semiconductor International*, 11(8):64 (1988)
17. Skidmore, K., *Semiconductor International*, 10(9):80 (1987)
18. Bean, K. E., in: *Semiconductor Materials and Process Technology Handbook for VLSI and ULSI*, (McGuire, ed.) p. 80, Noyes Publications, Park Ridge (1988)
19. Lang, G. A. and Stavish, T., *RCA Review*, 24:488 (1963)
20. Shepherd, W. H., *J. Electrochem. Soc.* 112:988 (1965)
21. Chu, T. L., Gruber, G. A. and Stickler, R., *J. Electrochem. Soc.* 113:156 (1966)
22. Dismukes, J. P. and Ulmer, R., *J. Electrochem. Soc.* 118:634 (1971)
23. Dismukes, J. P. and Levin, E. R., *Proc. Am. Inst. Chem. Eng.*, p. 135 (1970)
24. Reisman, A. and Berkenblit, M., *J. Electrochem. Soc.* 112:812 (1965)
25. Gregor, L. V., Balk, P. and Campagna, F. J., *IBM J. Res.* 9:365 (1965)
26. Ruzyllo, J., *Microcontamination*, 6(3):39 (1988)
27. Ruzyllo, J., *Solid State Technology*, 33(3):S1 (1990)
28. Ruzyllo, J., Frystak, D. C. and Bowling, R. A., in: *Proc. IEEE International Electron Device Meeting*, San Francisco, p. 409, (1990)
29. Ruzyllo, J., Hoff, A. M., Frystak, D. C. and Hossain, S. D., *J. Electrochem. Soc.* 136(5):1474 (1989)
30. Moghadam, F. K. and Mu, X.-C., *IEEE Transactions on Electron Devices*, 36(9):1602 (1989)



### 332 Handbook of Semiconductor Wafer Cleaning Technology

31. Fonash, S. J., *J. Electrochem. Soc.* 137(12):3885 (1990)
32. Ohmori, T., Fukumoto, T., Kato, T., Tada, M. and Kawaguchi, T., in: *First Intern. Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, (Ruzyllo and Novak, ed.) 90-9:182, The Electrochemical Society, Inc., (1989)
33. Sherman, R. and Whitlock, W., *J. Vac. Sci. Technol. B* 8(3):563 (1990)
34. Tabe, M., *Appl. Phys. Lett.* 45(10):1073 (1984)
35. Vig, J. R., *J. Vac. Sci. Technol. A* 3(3):1027 (1985)
36. Holmes, P. J. and Snell, J. E., *Microelectronics and Reliability*, 5:337 (1966)
37. Helms, C. R., Deal, B. E. and McNeilly, M. A., in: *1991 Proceedings*, p. 822, The Institute of Environmental Sciences, Mount Prospect, ILL (1991)
38. Helms, C. R. and Deal, B. E., in: *Fall Meeting Extended Abstracts*, 91-2, p. 807, The Electrochemical Society, Phoenix (1991)
39. Helms, C. R. and Deal, B. E., "Mechanisms of the HF/H<sub>2</sub>O Vapor Phase Etching of SiO<sub>2</sub>," to be published *J. Vac. Sci. Technol.*
40. Brosheer, J. C., Lenfesty, F. A. and Elmore, K. L., *Industrial & Eng. Chem.* 39:423 (1947)
41. Munter, P. A., Aepli, O. T. and Kossatz, R. A., *Industrial and Engineering Chemistry*, 39:427 (1947)
42. Munter, P. A., Aepli, O. T. and Kossatz, R. A., *Industrial and Engineering Chemistry*, 41(2):1504 (1949)
43. Thomsen, S. M., *J. Am. Chem. Soc.* 74:1690 (1952)
44. Whynes, A. L., *Trans. Instn Chem. Engrs.* 34:117 (1956)
45. Illarionov, V. V., Smirnova, Z. G. and Knyazeva, K. P., *Zhurnal Prikladnoi Khimii*.36(2):237 (1963)
46. Beyer, K. D. and Kastl, R. H., U. S. Patent 4,264,374 (April 28, 1981)
47. Blackwood, R. D., Biggerstaff, R. L., Clements, D. and Cleavelin, R., U. S. Patent 4,749,440 (June 7, 1988)
48. Bersin, R. L. and Reichelderfer, R. F., *Solid State Technology* 20(4):78 (1977)
49. Saito, Y., Yamaoka, O. and Yoshida, A., *Appl. Phys. Lett.* 56(12):1119 (1990)
50. Ibbotson, D. E., Mucha, J. A., Flamm, D. L. and Cook, J. M., *J. Appl. Phys.* 56(10):2930 (1984)
51. Skidmore, K., *Semiconductor International* 12(7):80 (1989)

52. Mishima, H., Ohmi, T., Mizuniwa, T. and Abe, M., *IEEE Transactions on Semiconductor Manufacturing* 2(4):121 (1989)
53. Mishima, H., Yasui, T., Mizuniwa, T., Abe, M. and Ohmi, T., *IEEE Transactions on Semiconductor Manufacturing* 2(3):69 (1989)
54. Oki, I., Biwa, T., Kudo, J. and Ashida, T., in: *Fall Meeting Extended Abstracts*, 91-2:790, The Electrochemical Society, Inc., Phoenix, Arizona (1991)
55. Syverson, D. J. and Duranko, G. T., *Solid State Technology* 31(10):101 (1988)
56. Cleavelin, D. C. R. and Duranko, G. T., *Semiconductor International* 10(11)(1987)
57. Novak, R. E., *Solid State Technology* 31(3):39 (1988)
58. Syverson, D., in: *1991 Proceedings*, p. 829, Institute of Environmental Sciences, Mount Prospect, IL (1991)
59. Deal, B. E., McNeilly, M. A., Kao, D. B. and deLarios, J. M., in: *Proceedings of the First International Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, (Ruzyllo and Novak, ed.) 90-9:121, The Electrochemical Society, Inc., (1989)
60. Deal, B. E., McNeilly, M. A., Kao, D. B. and deLarios, J. M., *Solid State Technology* 33(7):73 (1990)
61. Norton Co., 1. N. B. S., Worcester, MA 01615, U. S. Patent 4,761,134 (Aug. 2, 1988)
62. Nobinger, G. L., Moskowitz, D. J. and Krusell, W. C., "Vapor Phase Technology: Sensitivities and Uniform Etching of SiO<sub>2</sub>", to be published.
63. van der Heide, P. A. M., Baan Hofman, M. J. and Ronde, H. J., *J. Vac. Sci. Technol.* A7(3):1719 (1989)
64. Onishi, S., Matsuda, K. and Sakiyama, K., in: *Spring Meeting Extended Abstracts*, 90-1:519, The Electrochemical Society, Washington D.C. (1990)
65. Onishi, S., Matsuda, K. and Sakiyama, K., in: *Third International Symposium on Ultra Large Scale Integration Science and Technology*, (Andrews and Celler, ed.) 91-11:226, The Electrochemical Society, Inc., (1991)
66. Wong, M., Moslehi, M. M. and Reed, D. W., *J. Electrochem. Soc.* 138(6):1799 (1991)
67. Wong, M., Liu, D. K. Y., Moslehi, M. M. and Reed, D. W., *IEEE Electron Device Letters* 12(8):425 (1991)

### 334 Handbook of Semiconductor Wafer Cleaning Technology

68. Izumi, A., Matsuka, T., Takeuchi, T. and Yamano, A., in: *Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials*, p. 135, Japan Society of Applied Physics, Yokohama (1991)
69. Ehrlich, D. J., Osgood, R. M., Jr. and Deutsch, T. F., *Appl. Phys Lett.* 38(12):1018 (1981)
70. Okano, H., Horiike, Y. and Sekine, M., in: *Spring Meeting Extended Abstracts*, 83-1:673, The Electrochemical Society, Inc., San Francisco (1983)
71. Horioka, K., Okano, H. and Horiike, Y., in: *16th International Conference on Solid State Devices and Materials Final Program*, p. 50, Japan Society of Applied Physics, Kobe (1984)
72. Sugino, R., Nara, Y., Yamazaki, T., Watanabe, S. and Ito, T., in: *19th Conference on Solid State Devices and Materials*, p. 207, Japan Society of Physics, Tokyo (1987)
73. Sato, Y., Sugino, R., Okuno, M. and Ito, T., in: *22nd (1990 Intl.) Conference on Solid State Devices and Materials*, p. 1103, Japan Society of Physics, Sendai (1990)
74. Ito, T., Sugino, R., Watanabe, S., Nara, Y. and Sato, Y., in: *First International Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, (Ruzyllo and Novak, ed.) 90-9:114, The Electrochemical Society, (1989)
75. Ito, T. and Sugino, R., in: *Semiconductor World*, p. 120, (March, 1989)
76. Ogryzlo, E. A., Ibbotson, D. E., Flamm, D. L. and Mucha, J. A., *J. Appl. Phys* 67(6):3115 (1990)
77. Kern, W. and Deckert, C. A., in: *Thin Film Processes*, (Vossen and Kern, ed.) p. 401, Academic Press, New York (1978)
78. Mai, C. C. and Looney, J. C., *SCP and Solid State Technology* 9(1):19 (1966)
79. Judge, J. S., *J. Electrochem. Soc* 118:1772 (1971)
80. Harrap, V., in: *Semiconductor Si*, (Huff and Burgess, ed.) p. 354, The Electrochemical Society, (1973)
81. Deal, B. E. and Kao, D.-B., in: *Tungsten and Other Refractory Metals for VLSI Applications II*, (Broadbent, ed.) p. 27, Materials Research Society (1986)
82. Archer, R. J., *J. Electrochem. Soc.* 104:619 (1957)
83. Raider, S. I., Flitsch, R. and Palmer, M. J., *J. Electrochem. Soc.* 122:413 (1975)

84. Hattori, T., Takase, K., Yamagishi, H., Sugino, R., Nara, Y. and Ito, T., *Jpn. J. Appl. Phys.* 28(2):296 (1989)
85. Morita, M., Ohmi, T., Hasegawa, E., Kawakami, M. and Ohwada, M., *J. Appl. Phys.* 68(3):1272 (1990)
86. Graf, D., Grundner, M., Schulz, R. and Muhlhoff, L., *J. Appl. Phys.* 68(10):5155 (1990)
87. Ting, W., Hwang, H., Lee, J. and Kwong, D. L., *Appl. Phys. Lett.* 57(26):2808 (1990)
88. Olsen, J. E. and Shimura, F., *J. Vac Sci. Technol.* A7(6):3275 (1989)
89. Miki, N., Kikuyama, H., Kawanabe, I., Miyashita, M. and Ohmi, T., *IEEE Transactions on Electron Devices* 37(1):107 (1990)
90. Kern, W., Schnable, G. L. and Fisher, A. W., *RCA Review* 37(3):3 (1976)
91. Bean, K. E., *Thin Solid Films* 83:173 (1981)
92. Kikuyama, H., Miki, N., Saka, K., Takano, J., Kawanabe, I., Miyashita, M. and Ohmi, T., *IEEE Transactions on Semiconductor Manufacturing* 4(1):26 (1991)
93. Higashi, G. S., Becker, R. S., Chabal, Y. J. and Becker, A. J., *Appl. Phys. Lett* 58(15):1656 (1991)
94. Ubara, H., Imura, T. and Hiraki, A., *Solid State Communications* 50(7):673 (1984)
95. Grundner, M. and Jacob, H., *Appl. Phys. A* 39:73 (1986)
96. Yablonovitch, E., Allara, D. L., Chang, C. C., Gmitter, T. and Bright, T. B., *Physical Review Letters* 57(2):249 (1986)
97. Burrows, V. A., Chabal, Y. J., Higashi, G. S., Raghavachari, K. and Christman, S. B., *Appl. Phys. Lett.* 53(11):998 (1988)
98. Graf, D., Grundner, M. and Schulz, R., *J. Vac. Sci. Technol* A7(3):808 (1989)
99. Chabal, Y. J., Higashi, G. S., Raghavachari, K. and Burrows, V. A., *J. Vac. Sci. Technol. A* 7(3):2104 (1989)
100. Higashi, G. S., Chabal, Y. J., Trucks, G. W. and Raghavachari, K., *Appl. Phys. Lett.* 56(7):1990 (1990)
101. Haring, R. A. and Liehr, M., "Reactivity of a Fluorine Terminated Si Surface," to be published, *J. Vac. Sci. Technol.*
102. Helms, C. R., Johnson, N. M., Schwarz, S. A. and Spicer, W. E., *J. Appl. Phys.* 50(11):1979 (1979)
103. Hahn, P. O. and Henzler, M., *J. Appl. Phys.* 52(6):4122 (1981)

### 336 Handbook of Semiconductor Wafer Cleaning Technology

104. Hahn, P. O., Yokohama, S. and Henzler, M., *Surface Science* 142:545 (1984)
105. Hahn, P. O. and Henzler, M., *J. Vac. Sci. Technol.* A2(2):574 (1984)
106. Hahn, P. O., Grundner, M., Schnegg, A. and Jacob, H., *Applied Surface Science* 39:436 (1989)
107. Hahn, P. O., Grundner, M., Schnegg, A. and Jacob, H., *Semiconductor Silicon 1990*, (Huff, Barraclough and Chikawa, ed.) 90-7:296, Electrochemical Society, Inc., (1990)
108. Heyns, M. M., *Microcontamination* 9(4):29 (1991)
109. Ohmi, T., in: *Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials*, p. 481, Japan Society of Applied Physics, Yokohama (1991)
110. Offenbergs, M., Liehr, M. and Rubloff, G. W., *J. Vac. Sci. Technol.* A9(3):1058 (1991)
111. Batey, J., Tierney, E. and Nguyen, T. N., *IEEE Electron Device Letters* EDL-8(4):148 (1987)
112. Stasiak, J., Batey, J., Tierney, E. and Li, J., *IEEE Electron Device Letters* 10(6):245 (1989)
113. Batey, J., Tierney, E., Stasiak, J. and Nguyen, T. N., *Applied Surface Science* 39:1 (1989)
114. Miki, N., Maeno, M., Maruhasi, K. and Ohmi, T., *J. Electrochem. Soc.* 137(3):787 (1990)
115. Meieran, E. S., Flinn, P. A. and Carruthers, J. R., *Proc. of the IEEE* 75:908 (1987)
116. Hockett, R. S. and Katz, W., *J. Electrochem. Soc.* 136(11):3481 (1989)
117. Davis, L. E., Katz, W., Eberle, W. J. and Zazzera, L. A. *Microcontamination Conf. Proc.* (1989)
118. Phillips, B. F., Burkman, D. C., Schmidt, W. R. and Peterson, C. A., *J. Vac. Soc. Technol.* A1(2): 646 (1983)
119. Pool, R., *Science* 247:634 (1990)
120. Grosse, P., Harbecke, B., Heinz, B., Meyer, R. and Offenbergs, M., *Appl. Physics* A39:257 (1986)
121. Aspnes, D. E., in: ACS Symposium Series 295, *Microelectronic Processing: Inorganic Materials Characterization*, (Casper, ed.) p. 192, American Chemical Society, Washington DC (1986)
122. Shimazaki, A., in: *Defects in Silicon II*, (Bullis, Gosele and Shimura, ed.) 91-9:47, The Electrochemical Society, Inc., (1991)

123. Hahn, S., Eichinger, P., Park, J. G., Kwack, Y. S., Cho, K. C. and Choi, S. P., in: *Semicon/Korea Technical Proceedings*, p. 60, Semiconductor Equipment and Materials International, Seoul (1991)
124. Deal, B. E., in: *Proc. First Electronic Materials and Processing Congress*, p. 41, ASM International, Chicago (1988)
125. Menon, V. B., Clayton, A. C., Michaels, L. D. and Donovan, R. P., *Solid State Technology* 32(10):S9 (1989)
126. Bowling, R. A. and Larrabee, G. B., *J. Electrochem. Soc.* 136(2):487 (1989)
127. Onishi, S., Matsuda, K. and Sakiyama, K., A in: *22nd International Conference on Solid State Devices and Materials*, p. 1127, Japan Society of Physics, Sendai (1990)
128. Kasi, S. R., Liehr, M., Thiry, P. A., Dallporta, H. and Offenber, M., *Appl. Phys. Lett.* 58(1):106 (1991)
129. Kasi, S. R. and Kiehr, M., *Appl. Phys. Lett.* 57(20):2095 (1990)
130. Kaneko, T., Suemitsu, M. and Miyamoto, N., *Jpn. J. Appl. Phys.* 28:2425 (1989)
131. Zazzera, L. A. and Moulder, J. F., *J. Electrochem Soc.* 136(2):484 (1989)
132. Gluck, R. M., in: *Electrochemical Society Fall Meeting Extended Abstracts*, 91-2:759, Electrochemical Society, Phoenix (1991)
133. Ito, T., in: *1991 Proceedings*, p. 808, Institute of Environmental Sciences, Mount Prospect, Ill (1991)
134. Kubaschewski, O. and Alcock, C. B. *Materials Science and Technology*. (Raynor, ed.), Fifth Ed., Pergamon Press, Oxford (1983)
135. Ohsawa, A., Honda, K., Takizawa, R., Nakanishi, T., Aoki, M. and Toyokura, N., in: *Sixth International Symposium on Silicon Materials Science and Technology*, (Huff, Barraclough and Chikawa ed.) 90-7:601, The Electrochemical Society (1990)
136. Tamura, M., Isomae, S., Ando, T., Ohyu, K., Yamagishi, H. and Hashimoto, A., in: *Defects in Silicon II*, (Bullis, Gosele and Shimura, ed.) 91-9:3, The Electrochemical Society, Inc., (1991)
137. Iyer, S. S., Arienzo, M. and Fresart, E. D., *Appl. Phys. Lett.* 57:895 (1990)
138. Galewski, C., Lou, J.-C. and Oldham, W. G., *IEEE Transactions on Semiconductor Manufacturing* 3(3):93 (1990)
139. de Boer, W. B. and van der Linden, R. H. J., in: *Fall Meeting Extended Abstracts*, 91-2:808, The Electrochemical Society, Phoenix (1991)

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140. Deal, B. E., *J. Electrochem. Soc.* 127(4):979 (1980)
141. Kao, D. B., Cairns, B. R. and Deal, B. E., in: *Fall Meeting Extended Abstracts*, 91-2:802, The Electrochemical Society, Phoenix (1991)
142. Lo, G. Q., Ting, W., Kwong, D.-L., Kuehne, J. and Magee, C. W., *IEEE Electron Device Letters* 11(11):511 (1990)
143. Nishioka, Y., E. F. da Silva, J., Wang, Y. and Ma, T. P., *IEEE Electron Device Lett* 9:38 (1988)
144. Morita, M., Kubo, T., Ishihara, T. and Hirose, M., *Appl. Phys. Lett.* 45(12):1312 (1984)
145. Schwettmann, F. N., Chiang, K. L. and Brown, W. A., in: *Spring Meeting Extended Abstracts*, 78-1:688, The Electrochemical Society, Seattle (1978)
146. deLarios, J. M., Kao, D. B., Helms, C. R. and Deal, B. E., *Appl. Phys. Lett.* 54(8):715 (1989)
147. deLarios, J. M., "Effect of Aqueous Chemical Cleaning on the Si and Silicon Dioxide Surface and Silicon Oxidation Kinetics," Ph.D Dissertation, Stanford University (1989)
148. deLarios, J. M., Kao, D. B., Deal, B. E. and Helms, C. R., *J. Electrochem. Soc.* 138:2353 (1991)
149. Van Leeuwen, C., *Semiconductor International* 13(1):68 (1990)
150. Newboe, B., *Semiconductor International* 13(8):82 (1990)
151. Shankar, K., *Solid State Technology* 33(10):43 (1990)
152. Burggraaf, P., *Semiconductor International* 13(9):56 (1990)
153. McNab, T. K. P., *Semiconductor International* 13(9):58 (1990)
154. Bergendahl, A. S., Horak, D. V., Bakeman, P. E. and Miller, D. J., *Semiconductor International* 13(10):94 (1990)
155. McNab, T. K. P., *Semiconductor International* 13(11):86 (1990)
156. Bader, M. E., Hall, R. P. and Strasser, G., *Solid State Technology* 33(5):149 (1990)
157. Korolkoff, N. O., *Solid State Technology* 33(8):73 (1990)
158. Ohmi, T. and Shibata, T., *Microelectronic Engineering* 10:177 (1991)
159. Ohmi, T., *Microcontamination* 8(6):27 (1990)
160. Ohmi, T. and Shibata, T., *Microcontamination* 8(7):25 (1990)
161. Parikh, M. and Bonora, A. C., *Semiconductor International* 8(5):222 (1985)
162. Harada, H. and Suzuki, Y., *Solid State Technology* 29(12):61 (1986)

163. Liehr, M. and Kasi, S. R., in: *Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials*, p. 484, Japan Society of Applied Physics, Yokohama (1991)
164. Offenberg, M., Liehr, M., Rubloff, G. W. and Holloway, K., *Appl. Phys. Lett.* 57:1254 (1990)
165. Lucovsky, G., Kim, S. S., Fitch, J. T., Wang, C., Rudder, R. A., Fountain, G. G., Hattangady, S. V. and Markunas, R. J., *J. Vac. Sci. Technol.* A9(3):1066 (1991)
166. Pan, P., Berry, W., Kermani, A. and Liao, J., *Solid State Technology* 33(1):37 (1990)
167. Werkhoven, C. J., Westendorp, J. E. M., Huusen, F. and Granneman, E. H. A., *Semiconductor International* 14(6):228 (1991)
168. Zhou, Z.-H., Yu, F. and Reif, R., *J. Vac. Sci. Technol.* B9(2):374 (1991)
169. Kermani, A., Johnsgard, K. E. and Wong, F., *Solid State Technology* 34(5):71 (1991)



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## Silicon Surface Chemical Composition and Morphology

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*Gregg S. Higashi and Yves J. Chabal*

### 1.0 INTRODUCTION

The chemical state in which a surface is left subsequent to a clean is as important as the clean itself. A surface that becomes recontaminated before the next processing step will not be useful. The best cleaning techniques are therefore the ones which chemically *passivate* the semiconductor surface in the act of cleaning it.

There are two predominant ways to clean and passivate silicon surfaces chemically. The first is to grow a thin layer of oxide in the act of cleaning. This is best accomplished using acidic or basic solutions mixed with hydrogen peroxide and is the basis of the RCA Standard Clean developed by Kern in 1965 (1). These cleans leave 10-15 Å of hydroxylated oxide on the silicon surface which prevents recontamination of the silicon. Such surfaces are hydrophilic in nature and are easily wetted by aqueous solutions. The second way to clean and passivate the surface is to dissolve the surface oxide completely in hydrofluoric acid. Indeed, the early electronic measurements of Buck and McKim (1958) (2) demonstrated the high degree of passivation of HF-treated Si surfaces. These surfaces are now known to be oxide-free and passivated with hydrogen. The H-terminated surfaces are hydrophobic in nature and are *not* wetted by aqueous solutions. The body of this chapter is thus broken up into two parts: The surfaces produced by cleans that involve chemical oxidation (hydrophilic surfaces) are discussed in Sec. 2 and the surfaces produced by HF acid etching (hydrophobic surfaces) are discussed in Sec. 3.

The chemical composition of the silicon surface subsequent to a clean is fundamental to its passivation. The chemically grown oxides exhibit a more complex chemical composition than the high quality stoichiometric  $\text{SiO}_2$  grown thermally. Thermal oxides have been studied extensively because of their application as gate insulators in the MOS technology (Sec. 2.1). However, as gate oxide thicknesses decrease, the importance of the cleaning procedures employed is increasing, motivating in-depth studies of chemically grown oxides. Section 2.2 presents what is currently understood about the chemical composition of these hydrophilic surfaces.

The chemical composition of HF-etched silicon surfaces has been the subject of some confusion. It has long been held that the hydrophobic nature of these surfaces was explained by fluorine termination and that the surfaces were hydrophobic because they resembled Teflon™. In actuality, these surfaces are terminated with hydrogen and are therefore more paraffin-like due to the non-polar nature of the Si-H bond. Because of the confusion, a detailed history of the evidence for H-termination is presented in Sec. 3.1. A chemical mechanism which explains how the silicon surfaces become hydrogen-terminated is then described.

The micro-structural state of the surface has been shown recently to affect subsequent device properties (3)-(5). Surface roughness causes degradation of the breakdown field strengths of thin gate oxides (4)(5) and leads to decreased channel mobilities (3)(5). Both hydrophilic and hydrophobic surface cleans can affect the morphology of the Si surface and will be discussed separately in Sec. 2.3 and Sec. 3.2, respectively. Chemically grown oxides are non-crystalline, limiting the information obtained from most techniques for structural analysis. In contrast, HF etching leads to hydrogen termination of the bulk crystal and can be studied in great detail. In order to understand the variety of structures produced by different HF solution chemistries, the principles and limitations of the most useful structural analysis techniques are first briefly reviewed in Sec. 3.2. The huge differences observed between the surface structures of Si(100) and Si(111) wafers after HF etching are then discussed. In particular, the structural morphology on both surfaces varies with solution pH, favoring the formation of (111) facets at high pH. The mechanism of this preferential etching is presented in Sec. 3.2.

Contamination is also an important issue for any cleaning or passivation process because trace amounts of impurities can drastically influence subsequent materials properties. Contaminants can be intrinsic (e.g., H, OH,  $\text{H}_2\text{O}$ , F) or extrinsic (e.g., C, Fe, Ni, Cr, Cu) to the solutions used and

will be treated separately. Contamination issues for oxide-covered surfaces are discussed in Sec. 2.4. The contamination and the resulting loss of passivation of H-terminated surfaces are discussed in Sec. 3.3.

## **2.0 OXIDE-TERMINATED SURFACES**

### **2.1 Introduction**

As early as the 1950s, Atalla, Tannenbaum, and Scheibner (1959) (6) recognized the significance of oxide passivation of silicon semiconductor devices. Their discovery of the unique passivation properties of thermally grown oxides, which led to remarkable improvements in device performance, is a cornerstone of the modern silicon technology. It is noteworthy that the importance of surface chemical cleaning prior to oxidation was already being stressed. In particular, the distinction between cleans resulting in hydrophilic versus hydrophobic surfaces was noted, but not understood at that time. Although this chapter focuses on oxides grown chemically during cleaning, many analogies to the thermally grown oxides exist. Therefore, a brief discussion of the thermal oxides is useful to an overall understanding of these issues.

Thermally grown oxides have been characterized extremely well because of their technological significance. Entire books have been devoted to this subject (7)-(9), hence only a brief summary follows. Thermally grown oxides are formed by heating silicon wafers in either an  $O_2$  or an  $H_2O$  environment. The resulting oxide is a non-crystalline, stoichiometric, low defect density form of  $SiO_2$ . The  $SiO_2$  layer is largely impervious to contamination and protects the underlying Si substrate. A high degree of chemical passivation of the Si/ $SiO_2$  interface is observed in the electronic properties of the interface. "Dangling" bond densities below  $10^{11} \text{ cm}^{-2}$  are routinely achieved at the Si/ $SiO_2$  interface ( $10^{10} \text{ cm}^{-2}$  subsequent to  $H_2$  annealing) with fixed charged densities on the order of  $10^{10} \text{ cm}^{-2}$ . The electronic perfection of this interface is the basis of the MOS technology and may be related to the atomic order of the Si/ $SiO_2$  boundary.

Although the chemical perfection of the Si/ $SiO_2$  interface is well established, the molecular structure is less well understood. It is clear that there is a transition region between the bulk stoichiometric amorphous  $SiO_2$  and the crystalline Si substrate of 3 - 7 Å where suboxides are observed by XPS (10). It is less clear, however, what the exact structure and composition

are for this transition region. The various models proposed have recently been reviewed by Ourmazd and Bevk (1988) (11) and fall into three classes involving: a) An epitaxial  $\text{SiO}_2$  intervening layer; b) a disordered sub-stoichiometric oxide layer; and c) an abrupt transition directly from the crystalline Si to the continuous random network of amorphous  $\text{SiO}_2$ . Although the exact structure of the Si/ $\text{SiO}_2$  interface is still being debated, the transmission electron micrographs (TEM) of Ourmazd and Bevk (1988) (11) demonstrate that atomically flat interfaces can be obtained from atomically flat Si(100) starting surfaces.

Chemically grown oxides are produced by various cleaning techniques that are based on the use of acidic and/or basic hydrogen peroxide solutions. The most widely used system is the RCA Standard Clean developed by Kern and Puotinen (1970) (12). It is a sequential two-step clean where wafers are immersed first in a 5:1:1 solution of  $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{NH}_4\text{OH}$  at  $80^\circ\text{C}$  (SC-1) and then in a 5:1:1 solution of  $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$  at  $80^\circ\text{C}$  (SC-2). The Piranha etch, developed earlier, consists of an immersion in 4:1  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  at a temperature somewhat in excess of  $100^\circ\text{C}$ . Other cleans involve exposure to hot chemicals, such as nitric acid or other acid mixtures. The oxides left behind after these surface treatments are similar to the thermally grown oxides in some respects but are quite different in others. The discussion of these chemically grown oxides is divided up into three parts: chemical composition (Sec. 2.2), structural morphology (Sec. 2.3), and contamination issues (Sec. 2.4).

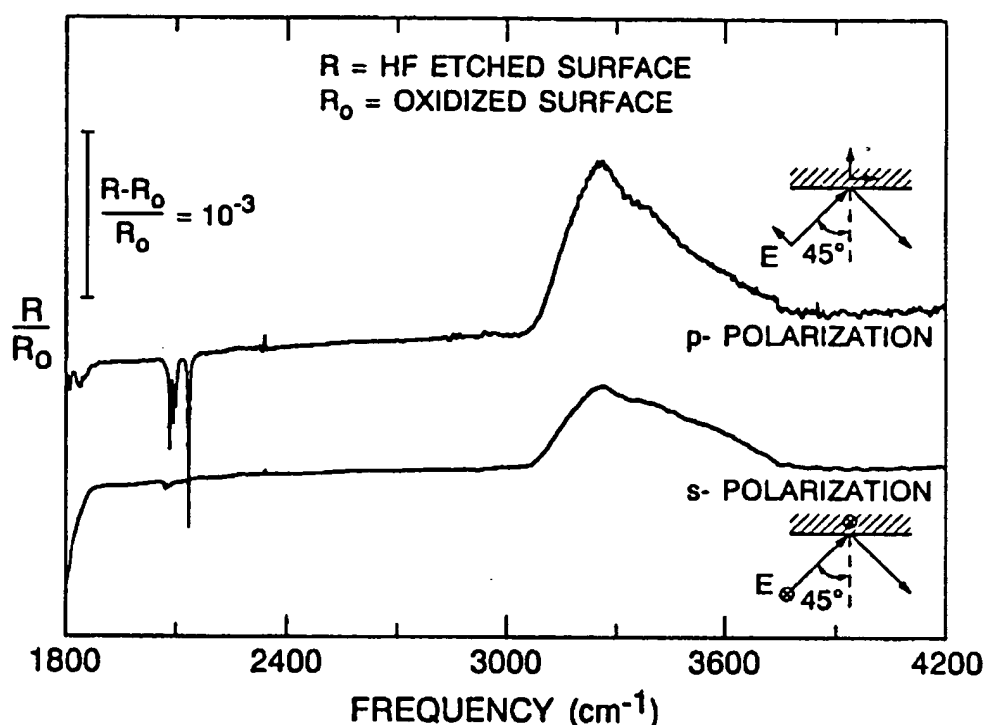
## 2.2 Chemical Composition

The properties of chemically grown oxides produced by the various cleaning techniques (Piranha etch, SC-1, or SC-2, etc.) are quite similar and have recently been reviewed by Deal (1987) (13). The oxides tend to be  $\sim 10$  -  $15 \text{ \AA}$  thick, depending on the process temperature as well as the solution chemistry used (14)(15). These films are largely stoichiometric but, because they are so thin, exhibit properties with many of the characteristics of the interfacial transition regions of thicker, thermally grown oxides. The large suboxide content characteristic of these chemically grown oxides is shown in the Si 2p core level spectra of Sugiyama et al. (1990) (16) in Fig. 1. For two different chemical preparations, the spectra are dominated by the Si crystal substrate ( $\text{Si}^0$ ) and by stoichiometric  $\text{SiO}_2$  ( $\text{Si}^{4+}$ ). There is, however, a relatively strong and unambiguous  $\text{Si}^{2+}$  contribution corresponding to an interfacial transition region similar to that observed for the thermal oxides. In this case, the  $\text{Si}^{2+}$  contribution is 10 - 20% that of the  $\text{Si}^{4+}$ ,



Chemical oxidation involves species other than Si and O. All aqueous solutions, of course, are predominantly composed of  $\text{H}_2\text{O}$  and are, therefore, sources of  $\text{H}_2\text{O}$ , OH and H. Thus, these chemical species must be incorporated in the oxide layer to some extent. There is an extensive literature on the infrared spectroscopy of OH and  $\text{H}_2\text{O}$  in and on the surfaces of silica glasses (18). These hydroxyl units are found in the form of Si-O-H or H-O-H. When the silica glasses are treated at elevated temperatures ( $\geq 550^\circ\text{C}$ ) under vacuum, a narrow ( $< 50\text{ cm}^{-1}$ ) infrared absorption band is observed at  $\sim 3750\text{ cm}^{-1}$ . This absorption is assigned to the O-H stretching vibration and is characteristic of isolated Si-O-H units. Without such a thermal treatment, the infrared absorption of the O-H stretch is extremely broad ( $\sim 400\text{ cm}^{-1}$ ) and peaks near  $3400\text{ cm}^{-1}$ , indicating a strong interaction between neighboring hydroxyl groups. This interaction, commonly referred to as hydrogen bonding, is simply a weak bonding between a hydrogen atom and an oxygen atom of neighboring molecules or molecular complexes. The exact nature of this bond is not completely understood. It is partially ionic and partially covalent and weakens the O-H bond, causing inhomogeneous broadening on the low frequency side of the isolated O-H stretching vibration. Hydrogen bonding is common to all aqueous solutions and is intimately related to the heat of solvation, as well as to the hydrophilic nature of oxide-covered Si surfaces.

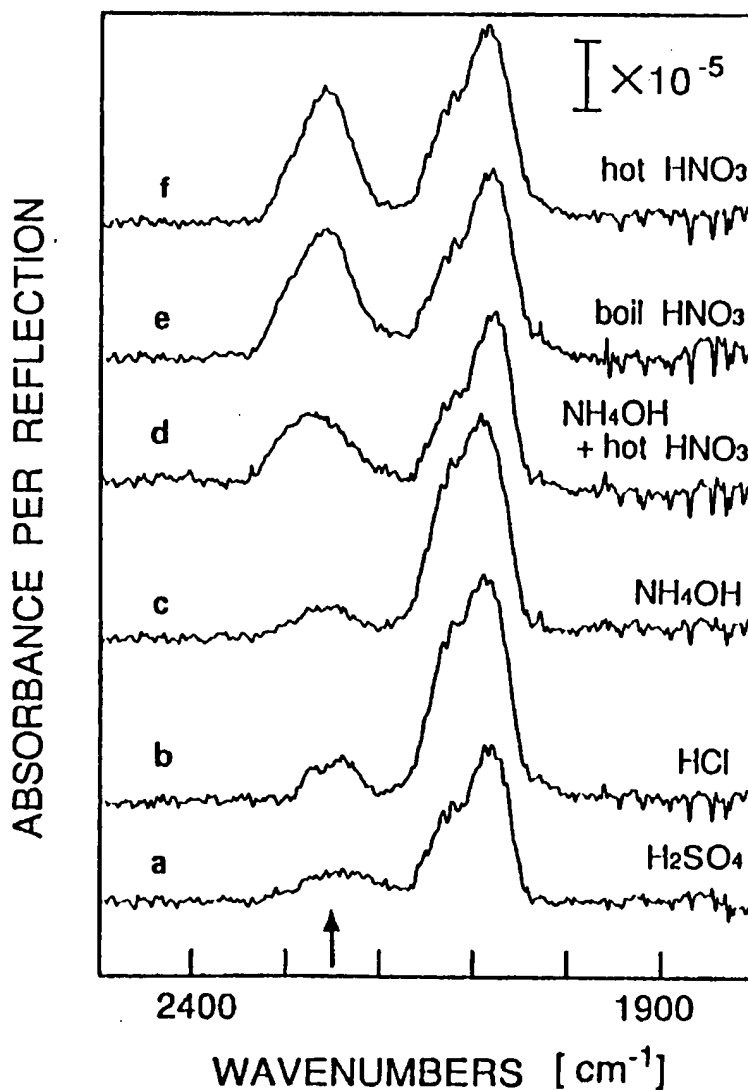
Hydrogen-bonded OH is observed on all chemically grown oxides. An example of an IR absorption spectrum of such a surface is shown in Fig. 2, where a hydrogen terminated silicon surface was chemically oxidized using the SC-2 step of the RCA clean. The spectra presented in Fig. 2 are ratios of oxidized and H-terminated silicon surfaces, and therefore display a negative absorption for the Si-H stretch bands ( $\sim 2100\text{ cm}^{-1}$ ) associated with the reference surface. The hydrogen bonded OH stretching vibration peaks at  $\sim 3300\text{ cm}^{-1}$  and is  $\sim 400\text{ cm}^{-1}$  wide (FWHM) with an asymmetric lineshape. It is quite difficult, however, to distinguish between Si-O-H and  $\text{H}_2\text{O}$  in these spectra without further spectral information from the scissor mode of the  $\text{H}_2\text{O}$  molecule in the  $1600 - 1700\text{ cm}^{-1}$  region. The intensity difference observed between the spectra taken in s- and p-polarizations indicates that the OH groups must reside in or on the oxide layer. Although it is unclear from these spectra, one knows in very general terms that most of the IR signal comes from  $\text{H}_2\text{O}$  on the surface of the oxide, since gentle heating ( $100^\circ\text{C}$ ) decreases the OH absorption substantially. Quantifying the amount of Si-O-H in and on the surface of these oxides is a direction for future research.



**Figure 2.** IR absorption spectra of silicon wafer chemically oxidized in a 4:1:1 solution of  $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$  at  $80^\circ\text{C}$  for 10 min. The spectra were ratioed to the corresponding spectra of the H-terminated silicon by etching in a buffered HF solution (see Ref. 89). A multiple internal reflection geometry was used with 75 reflections at a  $45^\circ$  internal angle of incidence, as shown in the inset.

It has now become apparent that Si-H units reside also on Si surfaces upon which chemical oxides have been grown (15)(16). The most convincing evidence comes from the IR spectra of Ogawa et al. (1992), (15) shown in Fig. 3, where Si-H stretching vibrations were identified at  $\sim 2260\text{ cm}^{-1}$ . Si-H stretches in that region of the spectrum originate from Si-H where the Si atom is back-bonded to O atoms (19). This evidence clearly indicates that the Si-H resides within the oxide matrix. The areal density is estimated to be  $2 - 3 \times 10^{13}\text{ cm}^{-2}$ . XPS data from the same group suggests that these Si-H units are actually localized near the surface of the oxide. If this is indeed the case, these units may be residual Si-H bonds from the original H-terminated hydrophobic surface before the chemical oxidation. This kind of picture agrees well with the idea that oxidation proceeds via O atom insertion between the Si-Si back-bonds of the surface and is consistent with the observations of Nagasawa et al. (1990) (20) on the initial stages of oxidation of hydrophobic surfaces. Also observed in the spectra of Fig. 3 are Si-H stretches in the range of  $2080\text{ cm}^{-1}$  which are best explained by H-

atoms bonded to substrate Si (i.e., back-bonded to Si atoms rather than to O atoms). The high frequency shoulder of this band ( $\sim 2140\text{ cm}^{-1}$ ) is most likely associated to Si-H stretches where some of the Si back-bonds are attached to an oxygen atom. If the mode at  $2080\text{ cm}^{-1}$  does arise from Si-H at the Si/SiO<sub>2</sub> interface, an interesting direction for future studies will be to determine its formation mechanism.



**Figure 3.** Infrared absorption spectra of six different native oxides on silicon wafers: (a) "H<sub>2</sub>SO<sub>4</sub>" corresponds to a 10 min treatment in 4:1 H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub> at 85 - 90°C, (b) "HCl", 10 min in 4:1:1 H<sub>2</sub>O:H<sub>2</sub>O<sub>2</sub>:HCl at 37 - 65°C, (c) "NH<sub>4</sub>OH", 10 min in 4:1:1 H<sub>2</sub>O:H<sub>2</sub>O<sub>2</sub>:NH<sub>4</sub>OH at 63 - 80°C, (d) "NH<sub>4</sub>OH + hot HNO<sub>3</sub>", in "NH<sub>4</sub>OH" followed by "hot HNO<sub>3</sub>". (e) "boil HNO<sub>3</sub>", in HNO<sub>3</sub> at 115 - 125°C, (f) "hot HNO<sub>3</sub>", 5 min in HNO<sub>3</sub> at 45 - 60°C. The absorption (indicated by the arrow) which peaks at  $\sim 2260\text{ cm}^{-1}$  arises from Si-H stretches where the Si is back-bonded to O (i.e. Si-H in or on the SiO<sub>2</sub>). (From Ref. 15.)



### **2.3 Structure and Morphology**

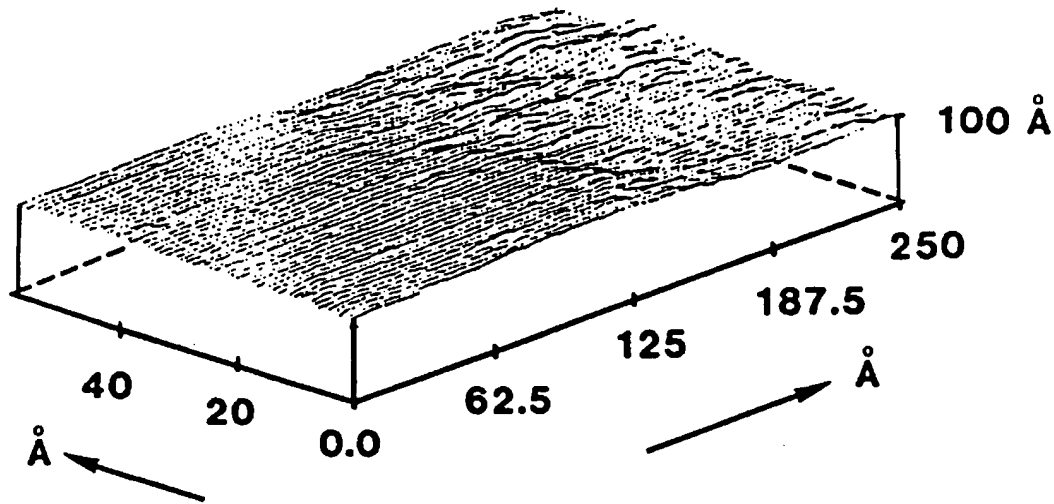
The work of Hahn and Henzler (1984) (3) and more recently of Heyns et al. (1989) (4) and Ohmi et al. (1991) (5) have correlated electronic device properties with surface structural properties. While it is intuitively obvious that surface roughness must be detrimental to semiconductor devices at some scale, the main contribution of these workers has been to define at what scale surface roughness is important to device yield and reliability. The evidence for degradation of thin gate oxide ( $<100 \text{ \AA}$ ) breakdown field strengths and channel mobilities with surface roughness on a microscopic scale is quite convincing and has captured the attention of the industry.

The morphology that a surface exhibits tends to be a function of the complete processing history experienced by the wafer; it is therefore quite complicated. The initial surface polish, any chemical cleaning, and processing steps such as thermal oxidation or any kind of etching all influence what the surface looks like. This section begins with a discussion of substrate wafers, including chemo-mechanical polishing and epitaxy. It then considers the effects of chemical cleans on surface morphology. Finally, future trends in controlling oxidation and interfacial structure are briefly discussed.

Near atomic perfection is achieved in surface chemo-mechanical polishing. Commercial wafers exhibit a typical surface roughness on the order of  $2 \text{ \AA}$  rms and surface finishes produced in the laboratory have approached  $1 \text{ \AA}$  rms (21). A scanning tunneling microscope (STM) image of such a surface is shown in Fig. 4. Although STM images can characterize surface roughness on length scales covering the range from one to a thousand angstroms, these surfaces were also characterized with a variety of other techniques spanning length scales up to  $1 \text{ mm}$  with good correlations observed on all length scales (21). The STM image shown in Fig. 4 was taken subsequent to removal of any surface oxide in HF, although chemo-mechanically polished wafers are hydrophobic and are already believed to be hydrogen-terminated (22). This process is not very well understood but will be discussed briefly in Sec. 3.1.

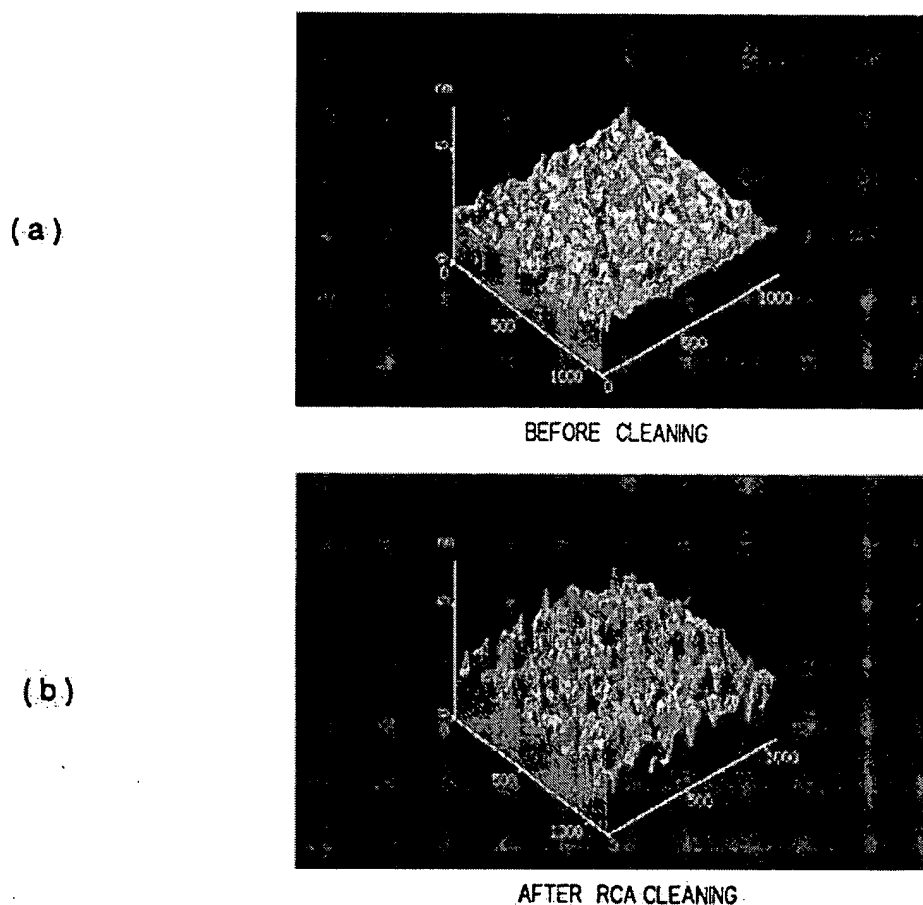
Hydrogen-terminated surfaces are not as stable as oxide-terminated surfaces, and thus it is not surprising that wafer vendors ship wafers in the hydrophilic (oxide covered) state. Vendor polishes and cleans are proprietary, but presumably the wafers receive something akin to an RCA clean before they are shipped. Another technique which provides atomically perfect surfaces uses Si molecular beam epitaxy, (23) although this

technique has not yet been commercialized. Surfaces formed during commercial Si epitaxial growth by chemical vapor deposition (CVD), however, might also be made atomically perfect under the proper conditions. Presently, as-received CZ-Si and epi-Si substrates seem to exhibit a surface roughness of  $\sim 2 \text{ \AA}$  rms (24).



**Figure 4.** Scanning tunneling microscope image of a polished Si(100) surface exhibiting  $1.2 \text{ \AA}$  rms roughness. The image was taken immediately following an HF dip. (Courtesy of P. O. Hahn, Wacker-Chemitronic GmbH, Germany, Ref. 21.)

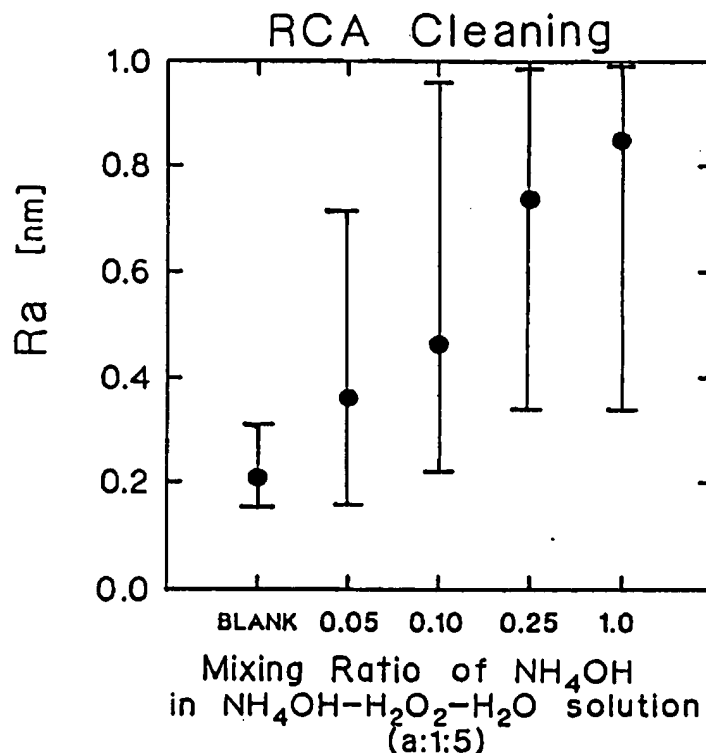
The consensus right now is that the acidic peroxide cleans (Piranha etch or SC-2) do not cause a substantial increase in the microscopic roughness of as-received wafers. The basic peroxide clean (typically 5:1:1  $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{NH}_4\text{OH}$  at  $80^\circ\text{C}$ ), on the other hand, has been found to substantially increase the surface roughness (25). A comparison of the surface roughness of a control wafer and a wafer cleaned in a standard SC-1 process is shown in the STM images of Fig. 5 (5). Control wafers exhibit an rms roughness of  $2 \text{ \AA}$ . The SC-1 treatment more than doubles the observed roughness and repetitive SC-1 cycles can increase it by as much as a factor of five, approaching  $10 \text{ \AA}$  rms. This kind of roughness has been shown to decrease breakdown field strengths by as much as 30% (26) and to degrade channel mobilities by factors of two to three (27).



**Figure 5.** Typical scanning tunneling microscope images of Si(100) surfaces taken before (a) and after (b) an RCA Standard Clean. Images taken after a newly developed buffered HF treatment where the authors observed minimal increases in surface roughness due to the BHF. (From Ref. 5.)

The mechanism leading to the roughening in the basic peroxide solution is not completely understood but is related to the slow but finite silicon etch rate in the SC-1 solution ( $\sim 8 \text{ \AA/min}$  at full strength at  $80^\circ\text{C}$ ) (5). The acidic peroxides, on the other hand, do not etch and hence do not roughen. A proposed solution to the basic peroxide roughening problem is to reduce the etch rate by reducing the concentration of  $\text{NH}_4\text{OH}$  in the SC-1 solution (25). The etch rate drops to  $1 \text{ \AA/min}$  if the concentration of  $\text{NH}_4\text{OH}$  is decreased by a factor of a hundred. Figure 6 shows a plot of the measured rms roughness as a function of  $\text{NH}_4\text{OH}$  concentration (28). One might wonder why the industry is working so hard to keep the standard SC-1 solution when it is clearly detrimental to the surfaces. The reason is simple:

SC-1 is one of the most efficient particle removal agents known. Further, the fact that the basic peroxide solution slightly etches both  $\text{SiO}_2$  and Si may be precisely why it is such an efficient particle remover. This phenomenon is being investigated in the hopes that an optimum concentration can be found to minimize damage and retain particle removal efficiency (5). The microscopic mechanism by which the etching roughens the surface is also being investigated. It should be mentioned that etching alone does not necessarily mean that the surface roughness will be increased. It is non-uniform etching which is really the culprit. For example, Verhaverbeke et al. (1991) (29) has found that the Ca concentration in the SC-1 dramatically changes the degree to which the surface roughens. Studies like these should be the direction of future work.



**Figure 6.** Surface roughness plotted as a function of  $\text{NH}_4\text{OH}$  concentration in a 10 min. ammonia-peroxide solution treatment at  $85^\circ\text{C}$ . (From Ref. 28.)

The exact molecular structure of these chemically grown Si/ $\text{SiO}_2$  interfaces is very difficult to deduce. In the past few years, however, "native" oxide growth has been shown to occur in an extremely controlled manner (23)(30), leading to atomically ordered interfaces under the right conditions. This phenomenon appears in fact to be more general. In very

Careful XPS studies of surface oxygen concentration as a function of time, layer by layer initial oxidation of Si has been observed (31)(32). Layer by layer oxidation, of course, requires that one layer finishes before the next layer begins oxidation and leads by necessity to the conclusion that some form of order must exist at the Si/SiO<sub>2</sub> interface.

## 2.4 Contamination Issues

One of the main objectives of the development of the RCA clean was to remove organic and metal contaminants from the surface of silicon wafers (1). Although the RCA clean was developed over twenty-five years ago, it has functioned extremely well and is still the dominant clean used prior to gate oxidation. As gate oxides move into the sub-100 Å regime, there has been renewed interest in how trace metal contamination in the pre-gate clean affects gate oxide properties (33). Residual trace metal contamination at the 10<sup>10</sup> cm<sup>-2</sup> level is observed after RCA cleaning, depending on the quality of the chemicals used and is discussed in detail in Ch. 12. It seems as though metals can get trapped in the oxide formed during the SC-1/SC-2 cleaning process. These metals can subsequently lead to leaky junctions and to yield and reliability problems in gate oxides (33)(34). It is beyond the scope of this discussion to address this issue further, but the reader should understand that the industry needs to be concerned with how cleaning is to be handled in the future.

Another common contaminant on these oxide covered surfaces is carbon. It is most likely incorporated in or on these surfaces in the form of hydrocarbons and can come from the chemicals, the water used to rinse the wafers, or from the air in the laboratory environment. Trace hydrocarbons have not proven to be detrimental to gate oxides. A predominant sentiment in the industry is that the hydrocarbons get "burnt" off in the oxygen-rich high-temperature environment of the oxidation furnace. If handled improperly, however, SiC precipitates can cause weak spots in the oxides grown (35).

Hydrocarbon contamination is much more of a concern for surface preparation prior to epitaxial growth of silicon. In this case, surfaces that are completely free of contamination are needed to grow defect free Si and carbon contamination is of critical concern. The technique of desorbing the oxide at elevated temperature prior to epitaxy was first discussed by Henderson (1972) (36) where he showed that atomically clean surfaces with only a small carbon residue could be obtained after the RCA Standard Clean. Ishizaka, Nakagawa and Shiraki (1982) (37) reduced the level of

carbon entrained in the oxide by repetitively immersing the wafers in boiling  $\text{HNO}_3$  acid followed by HF, ending with a concentrated SC-2 type of clean (3:1:1  $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  at 90 - 100°C). Another technique which is extremely efficient at removing hydrocarbons is UV-ozone (38) and is discussed in detail in Ch. 6.

Some contaminants, such as S and Cl, can originate directly from the solution used during the chemical oxidation. S and Cl have been observed from the Piranha and SC-2 cleans, respectively (see Ch. 12). Fluorine, on the other hand, has been observed when the chemical oxidation is preceded by an HF treatment. In this case, F is found to segregate at the Si/SiO<sub>2</sub> interface (39).

### 3.0 HYDROGEN-TERMINATED SURFACES

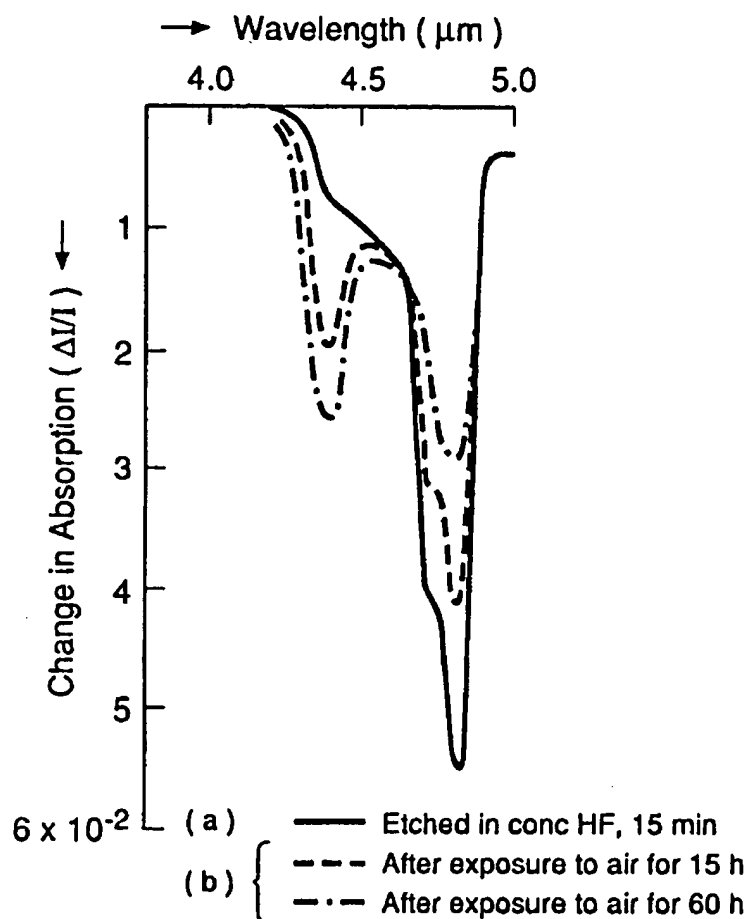
#### 3.1 Chemical Composition of HF Treated Surfaces (Wet)

**Historical Overview.** The unique properties of Si surfaces treated in HF solutions were recognized over thirty years ago, (2)(6) but only recently have these hydrophobic surfaces begun to be understood. It is now quite clear that *hydrogen* and *not fluorine* termination of the dangling bonds on the Si surface explains the hydrophobicity, the high resistance to chemical attack, and the low surface recombination velocity. Fluorine is also found on these surfaces, but only in small quantities and should be thought of as a minor contaminant rather than a major constituent of the surface. At first glance it is difficult to understand why the confusion and controversy about H vs. F termination took so long to sort out. The reader should understand, however, that most conventional surface spectroscopic methods (AES, XPS, etc.) rely on core electrons and cannot measure hydrogen, since it has no core. Thus, researchers tended to concentrate on those things they could detect rather than those they could not. Vibrational spectroscopies (EELS, IR, etc.), on the other hand, are extremely sensitive to hydrogen-containing surface species but have only begun to see widespread use in surface science during the last ten years. Because there has been so much confusion regarding this issue, a detailed experimental chronology of HF treated Si surfaces is presented in the following.

It is remarkable that, as early as 1965, Beckmann (40) had investigated the chemical properties of "stain films" with infrared absorption spectroscopy. Stain films were prepared electrochemically by anodic polarization in a 10 N aqueous solution of HF acid. They could be grown as

thick as 20 - 50  $\mu\text{m}$  and thus could be studied using *transmission* infrared absorption spectroscopy. A thorough investigation with deuterated solutions clearly identified hydrogen as the main chemical species in the films, mostly as pure hydrides  $\text{Si-H}_x$  and also as hydrides with silicon back-bonded to oxygen (of the form  $\text{O-Si-H}$ ), characterized by silicon-hydrogen stretching vibrations in the  $2100\text{ cm}^{-1}$  and the  $2275\text{ cm}^{-1}$  regions, respectively. Beckmann also assigned all the absorption bands measured in the lower frequency region ( $400 - 1100\text{ cm}^{-1}$ ). In particular, the presence of an absorption band at  $910\text{ cm}^{-1}$  made him consider fluorine, since it could be assigned to the  $\text{Si-F}$  stretch mode. This band, however, disappeared upon deuteration, casting serious doubts on the  $\text{Si-F}$  stretch assignment; the  $\text{Si-F}$  stretch has more recently been observed at  $\sim 800\text{ cm}^{-1}$  instead of  $910\text{ cm}^{-1}$  (41). However, Beckmann cautiously concluded that fluorine contamination could not be ruled out altogether because a strong interaction could result from the existence of several normal modes in the  $910\text{ cm}^{-1}$  range: the deformation vibrations of  $\text{SiH}_2$  and  $\text{SiH}_3$ , as well as the  $\text{SiF}_x$  stretch modes. He made a more positive identification of  $\text{OH}$  and a variety of silicon oxides in his spectra. Although the hydrocarbon region could not be studied because of the spectrometer, it is likely that the stain films had a substantial carbon concentration.

Almost ten years later, Harrick and Beckmann (1974) (42) reported on an infrared absorption study of silicon *dipped* in an  $\text{HF}$  solution (not *electrochemically* prepared as the stain films). The spectra, recorded with an internal reflection geometry (180 reflections), are summarized in Fig. 7. They are characterized by a spectral signature that is very similar to that observed in stain films, namely a strong  $\text{Si-H}_x$  stretch band with evidence for some oxygen present in the back-bond of the surface silicon atoms. Based on a comparison with the data on stain films, Harrick and Beckmann concluded that the layers formed by  $\text{HF}$  solution dipping were  $20\text{ \AA}$  thick on average. With today's knowledge, as will be shown in the next section, their spectra actually correspond to a monolayer coverage of an *atomically rough* surface, possibly with a  $20\text{ \AA}$  scale roughness. Although only the  $2000 - 2200\text{ cm}^{-1}$  spectral region was reported, it is likely that the surface contained carbon in addition to hydrogen and oxygen, due to relatively dirty chemicals used at the time. Regardless of the contamination issue, however, this was a clear indication that  $\text{HF}$  etched surfaces were terminated with hydrogen. This work was unfortunately either *buried* in the wrong literature or *ignored* because Harrick and Beckmann mistakenly assigned the  $\text{Si-H}$  stretching vibration they observed to an  $\text{Si-H}$  polymer deposited on the surface of the wafer.

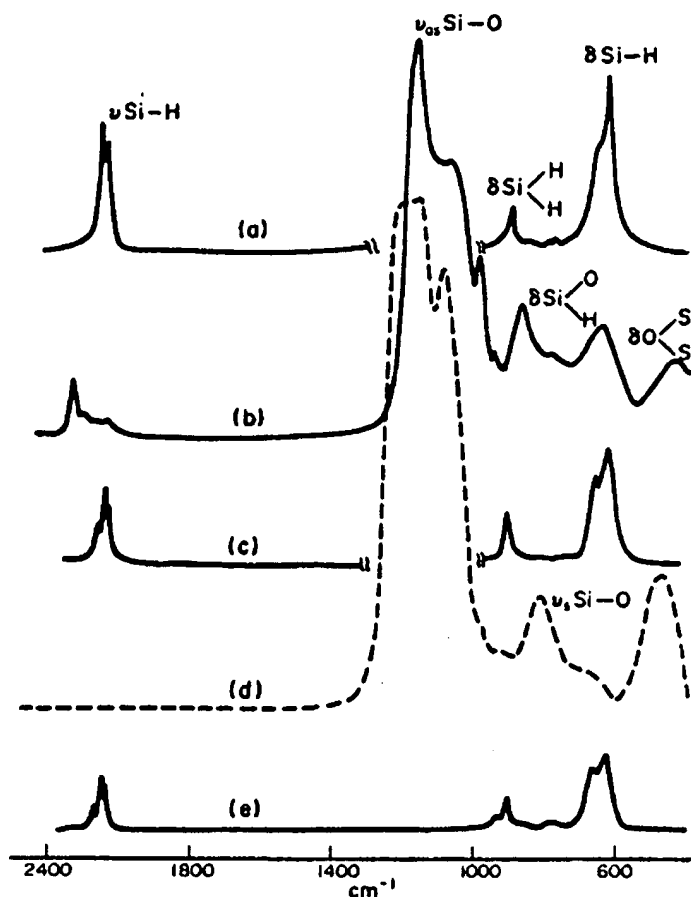


**Figure 7.** Multiple internal reflection (180 reflections,  $\theta_{\text{internal}} = 45^\circ$ ) IR absorption spectra of Si surfaces after (a) HF etching in 10 N solution, and (b) subsequent exposure to air for 15 h (dashed line) and for 60 h (dash-dotted line). The main absorption peak for freshly etched Si (solid spectrum) at 4.75  $\mu\text{m}$  ( $\sim 2100\text{cm}^{-1}$ ) is characteristic of H-termination of Si. The absorption band developing around 4.4  $\mu\text{m}$  ( $\sim 2250 - 2300\text{cm}^{-1}$ ) upon oxidation in air is characteristic of Si-H with oxygens in the Si-Si back-bonds. (From Ref. 42.)

In 1984, Ubara, Imura and Hiraki (1984) (43) also clearly showed that the removal of silicon oxide in HF solutions results in the formation of silicon hydrides. Their results obtained on hydrogenated microcrystalline silicon ( $\mu\text{c-Si:H}$ ) (44)(45), are summarized in Fig. 8. The as-grown samples (a) are thermally oxidized at low temperature (b), then HF solution etched (c), reoxidized at much higher temperature (d), and finally HF solution etched (e). The main result is best summarized in curves (d) and (e). After the high temperature thermal oxidation in air at  $600^\circ\text{C}$ , all traces of hydrogen have



disappeared (see curve d), as evidenced by the absence of the  $\text{SiH}_x$  bands centered at  $2100\text{ cm}^{-1}$ . This treatment clearly produced strong  $\text{Si-O}$  and  $\text{Si-O}_2$  bands centered at  $1100\text{ cm}^{-1}$ , confirming the formation of an oxide layer. Subsequent dipping in HF solution eliminated all the bands associated with silicon oxide and gave a spectrum with prominent silicon-hydrogen bands at  $2100\text{ cm}^{-1}$  ( $\text{SiH}_x$  stretch),  $900\text{ cm}^{-1}$  ( $\text{SiH}_2$  scissor), and  $650\text{ cm}^{-1}$  ( $\text{SiH}_x$  bends) (see curve e). These data clearly show the removal of silicon oxide in HF with subsequent termination of the surface by hydrogen. Ubara et al. (1984) (43) postulated a mechanism to account for the hydrogen termination, which was later confirmed by ab-initio calculations (46) and will be discussed in detail later in this section.



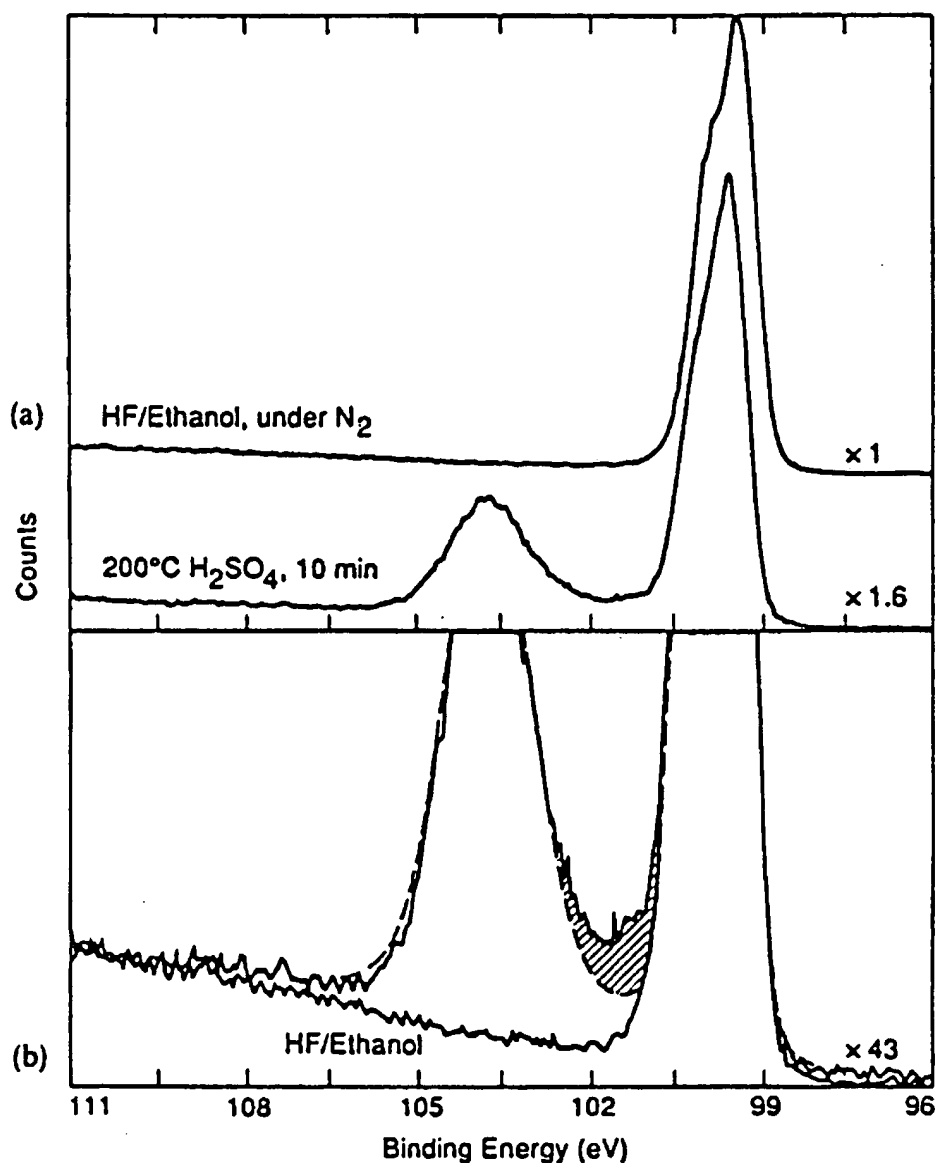
**Figure 8.** Transmission infrared absorption spectra of hydrogenated microcrystalline silicon ( $\mu\text{c-Si:H}$ ): (a) as grown using RF-reactive sputtering in  $\text{H}_2$  at  $250^\circ\text{C}$ , (b) after thermal oxidation in air at  $200^\circ\text{C}$  for 5 h, and (c) after subsequent HF etching of the previously oxidized surface; (d) after a thermal oxidation at  $600^\circ\text{C}$  for 1 h, and (e) subsequent HF etching of this previously thermally oxidized surface. (From Ref. 43.)

Despite these early pieces of work clearly pointing to hydride formation upon HF solution etching, it was still widely believed that fluorine was in fact the passivating agent. Raider et al. (1975) (47) attributed the hydrophobic nature of HF-etched surfaces to the presence of Si-F bonds or adsorbed HF. Licciardello et al. (1986) (48), indicated that the presence of an organic (hydrophobic) overlayer and not the Si-F surface per se was responsible for the hydrophobicity, although they still assumed that this overlayer was deposited on top of the *F-terminated* silicon surfaces. In addition, Weinberger et al. (1985) (49) explained the electronic passivation of HF-treated Si wafers as being due to fluorine termination of the Si dangling bonds. They further argued that the strength of the Si-F bond would make it an extremely stable surface, a point which will be discussed further in this section. Indeed, indirect support for F-passivation was drawn from the observation that F is a stable adsorbate on the surfaces of silicon prepared in UHV (41). Furthermore, fluorine was directly identified by XPS on HF-treated silicon surfaces, (50) suggesting that a monolayer of fluorine is present at the surface.

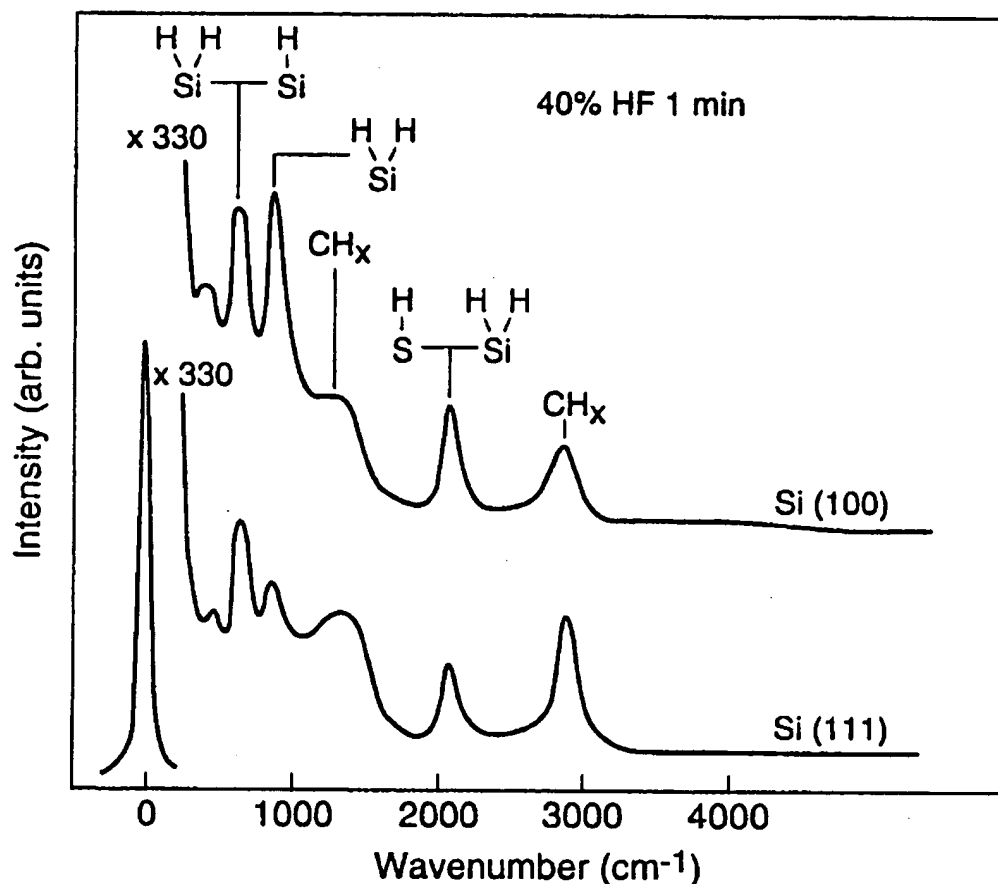
The year of 1986 was perhaps the turning point in the H- vs. F-termination debate. Yablonovitch et al. (1986) (51) observed that the F concentration, as measured by XPS, was highly variable and could not be the correct explanation for the remarkable surface passivation achieved subsequent to HF etching. Using infrared spectroscopy, they showed that a monolayer of hydrogen was adsorbed on the surface of HF-etched Si, with a spectrum characteristic of clean Si-H bonds (i.e., without oxygen or fluorine as a nearest neighbor). Another clear demonstration of the variability of the fluorine concentration on the surface came from the XPS data of Grunthaner and Grunthaner (1986) (52) showing no detectable oxygen, fluorine, nitrogen, or sulfur on HF/ethanol spin-etched silicon samples. Figure 9, for instance, shows the Si 2p core level spectra measured after different chemical treatments. The spin etched samples are characterized by an unshifted Si 2p core level, making it possible to set an upper limit of 0.1% of a monolayer of Si directly bonded to electronegative elements, such as fluorine or oxygen, for the spin-etched samples (53).

Independently, Grundner and Jacob (1986) (54) published the results of detailed EELS and XPS studies of oxidized and HF-etched silicon surfaces. The EELS data, shown in Fig. 10, consistently showed strong hydrogen vibrations at  $2100\text{ cm}^{-1}$ ,  $900\text{ cm}^{-1}$  and  $650\text{ cm}^{-1}$ , although hydrocarbons ( $2800\text{ cm}^{-1}$ ) and OH ( $3400\text{ cm}^{-1}$ ) vibrations contributed also to the spectra (55). The intensity of the fluorine 1s line measured in XPS

data (55)(56) indicated that the fluorine concentration, after a de-ionized water rinse, was always less than 1 - 2% monolayer. This work clearly confirmed the formation of silicon hydrides upon HF etching and suggested that fluorine was a contaminant that could be removed by rinsing in water.

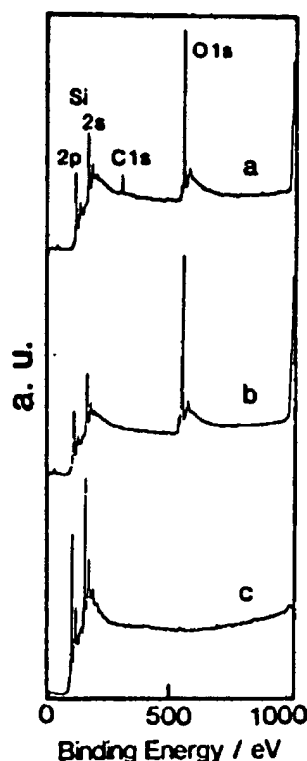


**Figure 9.** (a) Typical x-ray photoelectron spectra of the Si 2p core level obtained before (lower spectrum) and after (upper spectrum) a spin-etch in  $N_2$  by using HF in ethanol. (b) Expansion and overlay of the data shown in (a) to emphasize the region between the peaks that correspond to the Si substrate and to the  $SiO_2$ . The dashed line represents a least-square fit to these two major components. The cross-hatched region corresponds to Si suboxide species. (From Ref. 53.)



**Figure 10.** Electron energy loss spectra of Si(100) and Si(111) surfaces after 1 min. immersion in 40% HF solution (no rinsing) and subsequent introduction into UHV. The assignment of the main observed losses is summarized schematically above the spectra. (From Ref. 55.)

Both the surface-recombination velocity measurements of Yablonovitch et al. (1986) (51) and the extensive XPS and EELS studies of Grundner et al. (54)(55) motivated a number of photoelectron emission and infrared absorption studies (57)-(60). Takahagi et al. (1988) (57) used XPS, UPS and IR absorption to quantify the chemical species on the silicon surface after a combination of UV/ozone cleaning and HF dipping. Using dilute HF solutions, they achieved low levels of contamination (totaling less than 5% of a monolayer of O, C and F) and detected both Si-H and Si-H<sub>2</sub> species on the Si(100) surface. A typical XPS survey scan is shown in Fig. 11, which emphasizes the chemical purity of HF cleaned surfaces.



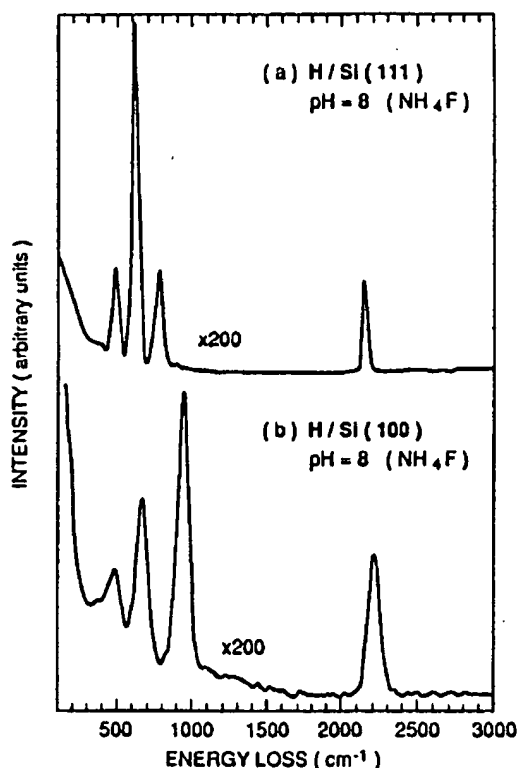
**Figure 11.** XPS Survey scan spectra of Si wafer surfaces (a) before UV-ozone cleaning (as purchased with 7Å thick native oxide and a 2Å thick organic contamination), (b) after UV-ozone cleaning with a low-pressure mercury lamp (184.9 nm and 253.7 nm emission) in an oxygen atmosphere, and (c) after subsequent HF dipping of the UV-cleaned sample in a 1% HF solution. (From Ref. 57.)

Burrows et al. (1988) (58) and Chabal et al. (1989) (59) investigated the silicon-hydrogen stretch vibrations ( $2000 - 2200 \text{ cm}^{-1}$  region) to quantify the surface morphology of silicon etched in dilute HF (no rinsing) and kept in a purged environment. The spectra for both Si(100) and Si(111) surfaces displayed a variety of hydrides (mono-, coupled mono-, di- and tri-hydrides) consistent with atomically rough surfaces covered with roughly one monolayer of hydrogen, discussed in detail later in this chapter. Although no detectable absorption bands were observed in the O-H stretch ( $3600 \text{ cm}^{-1}$ ) and  $\text{CH}_x$  stretch ( $2800 \text{ cm}^{-1}$ ) region, the sensitivity of these IR absorption measurements only placed an upper limit of 10% monolayer (ML) for these species.

Fenner et al. (1989) (60) applied much more sensitive techniques (XPS and AES) for the detection of C, O, F and N to samples prepared by various wet-chemical techniques, cleaving in UHV, and ion sputtering. They found that, among the various wet-chemical techniques, spin-etched samples with

HF-alcohol mixtures (HPLC grade) exhibited the lowest contamination levels (0.03 ML C, and 0.005 ML O and F), close to levels found on cleaved Si in UHV. By comparison, samples dipped in HF solutions or sputtered and annealed showed a tenfold increase in surface residue.

Very recently, Dumas and Chabal (1991,1992) (61)(62) have used Energy Electron Loss Spectroscopy (EELS) to characterize silicon surfaces etched in buffered HF solutions. For samples rinsed in de-ionized water after the etching, they find that the concentrations of impurities, such as Si-F, Si-C, Si-O, Si-OH and Si-CH<sub>x</sub>, are less than 1% of a monolayer (see Fig. 12). All losses in the EEL spectra can be assigned to hydrogen or silicon vibrations (61). This is in contrast to the early EELS data (55) (see Fig. 10) where relatively intense losses around 800 - 1100 cm<sup>-1</sup> (oxide) and around 2900 cm<sup>-1</sup> (hydrocarbons) were apparent. Possible reasons for the discrepancy are (a) variations in the purity of the chemicals used, (b) the exact handling and rinsing procedures, and (c) the wafer introduction and evacuation procedures used for these UHV studies.



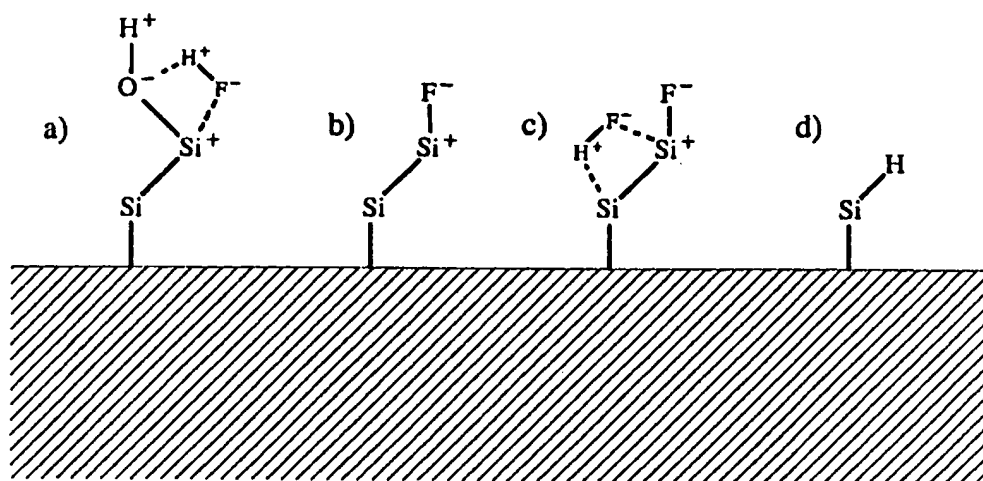
**Figure 12.** Electron energy loss spectra of (a) Si(111) and (b) Si(100) after etching in an ammonium fluoride solution (NH<sub>4</sub>F, pH = 7.8) and a brief (~10 sec) rinsing in DI water. The x200 factor corresponds to the magnification of the spectrum relative to the elastic peak. (From Ref. 61.)

The main conclusion of the above studies is that hydrogen acts as the passivating agent and is the direct result of HF etching. The concentration of contaminants, such as carbon, oxygen and fluorine, depends on the details of processing. In particular, the rinsing procedure after the last etching step directly affects the concentrations of fluorine and oxygen.

**Mechanism of Hydrogen Termination.** Part of the confusion concerning fluorine termination of the Si following HF etching has arisen not only because of the stability of the Si-F bonds, but because the accepted explanation of the mechanism for SiO<sub>2</sub> dissolution leads automatically to fluorine terminated Si. The dissolution of SiO<sub>2</sub> by HF can be depicted in its simplest form in the following reaction:



Notice that the above reaction involves HF molecules and not F<sup>-</sup> ions in the solution. HF is a weak acid having an equilibrium constant such that it does not dissociate readily in concentrated solutions (63). In addition, Judge (1971) (63) showed clearly that even if F<sup>-</sup> ions are available, they have an etch rate which is negligible compared to HF and HF<sub>2</sub><sup>-</sup> species. Thus, only HF in its associated form need be considered in the dissolution mechanism. HF molecules attack Si-O bonds by inserting themselves between the Si and O atoms. This reaction is depicted schematically in Fig. 13a as if it were the last Si-O bond to be broken before reaching the Si substrate. This insertion occurs with a low activation barrier because the reaction is highly exothermic and conserves the number of broken and reformed bonds. The reaction is also greatly facilitated by the highly polar nature of the Si-O bond, which the highly polar HF molecule can use to its advantage during attack. The Coulomb attraction naturally leads to having the positively charged H-atom associated with the negatively charged O-atom, and the negatively charged F-atom associated with the positively charged Si-atom of the Si-O bond. This liberates H<sub>2</sub>O into the solution and leaves Si-F in its place on the surface (Fig. 13b). The Si-F bond is the strongest single bond known in chemistry with a bond energy of ~6 eV. The bond strength of the Si-H is only ~3.5 eV and leads one, based on these thermodynamic considerations, to conclude that the F-terminated surface must be more stable than the H-terminated surface.



**Figure 13.** Schematic representation of silicon etching and hydrogen passivation by HF.

Ubara, Imura and Hiraki (1984) (44) were the first to propose a reaction mechanism to get around this dilemma. They recognized that the Si-F bond must be highly polar because of the large electronegativity difference between these atoms. They suggested that the Si-F bond causes bond polarization of the Si-Si back-bond allowing HF attack of the back-bond, as illustrated in Fig. 13c. This kinetically favorable pathway results in the release of stable  $\text{SiF}_x$  species into the solution leaving Si-H behind on the surface, as shown in Fig. 13d. The validity of this proposed pathway was confirmed using first principles molecular orbital calculations of the activation energies of these types of reactions on model compounds by Trucks et al. (1990) (46). In these calculations, an activation energy of  $\sim 1.0$  eV was found for reactions of the type shown in Fig. 13c. Low activation energies such as these are due to the charge transfer between the silicon and fluorine atoms, as originally suggested by Ubara et al. (44). In the absence of charge transfer, as is the case for the nonpolar Si-H bonds, the activation energy of the Si-Si back-bond attack is 1.6 eV, which is 0.6 eV higher in energy than for that of fluorinated Si species. The impact of the Coulomb interaction could also be observed by inverting the HF molecule, making the attack occur in opposition to the Coulomb force. In that case, an activation energy of 1.4 eV is obtained. In summary, HF attacks polar species very effectively but is much less effective against nonpolar species. Also, the reactant must attack the bonds in a specific orientation to take advantage of the Coulomb interaction between the positively and negatively charged atoms. These concepts allow us to understand why it is hydrogen and not fluorine that terminates the Si dangling bonds after HF solution etching, and why HF dissolves oxide so readily but leaves the Si relatively untouched.



The preceding arguments give us a basic understanding of HF etching. In reality, however, the situation is much more complex, with HF,  $\text{HF}_2^-$ ,  $\text{F}^-$ ,  $\text{H}_3\text{O}^+$ ,  $\text{OH}^-$ ,  $\text{NH}_4\text{F}$  species together in the solution, in chemical equilibrium with one another, not to mention the steric constraints at the surface or the effects of solvation on the reactions. A complete understanding of the detailed chemistry is not available at this time, but certain conjectures can be made with a reasonable degree of confidence. The calculations mentioned above were performed for molecules in free space and thus can accurately describe only gas phase reactions. We know, however, that water vapor is needed to initiate  $\text{SiO}_2$  etching reactions with anhydrous HF (64). One can argue that the main effect of placing the polar HF molecule into water is to surround it, on the average, with water molecules in the proper orientation to minimize the Coulomb energy. This, in turn, weakens the H-F bond, facilitating all HF reactions that must break the HF bond. One can, therefore, postulate that solvation simply lowers the activation barriers that exist for the gas phase reactions described above. Reaction rate data are not available for the Si-Si back-bond attack, but HF dissolution of  $\text{SiO}_2$  has an activation energy of approximately 0.35 eV (63), to be compared with the 0.55 eV calculated for the gas phase reaction (46). The heat of solvation to place an HF molecule into solution is  $\sim 0.4$  eV and is consistent with the observed 0.2 eV lowering of the energy barrier. This point of view also allows one to rationalize the HF and  $\text{HF}_2^-$  etching behavior observed by Judge (1971) (63). One can think of  $\text{HF}_2^-$  simply as a more highly solvated form of HF with a weaker bond strength that explains the lower activation energy for  $\text{SiO}_2$  dissolution (0.31 eV) as well as the increased rate of dissolution (factor of 4 - 5). The question of steric hindrance at the surface will be discussed in a later section. In general terms, confidence should be placed on the chemical trends discussed above while remaining skeptical of the exact activation energies, since modifications due to steric constraints or solvation can be expected.

One last point needs to be clarified regarding HF solution chemistry. It is now clear that the  $\text{OH}^-$  concentration has a drastic effect on the etching that occurs with HF solutions (65). Experiments show that water rinsing alone can remove dihydride species at steps (65)(66) and leads to monohydride termination on Si(111) surfaces (66). In this regard early workers noticed that samples which were rendered hydrophobic in HF remained so even after boiling in water for extended periods of time (6). It is equally curious that chemo-mechanically polished silicon wafers (polished in slurries with  $\text{pH} \leq 13$ ) are hydrophobic and are terminated with hydrogen (22). These observations taken together suggest that Si surface reactions with  $\text{OH}^-$  can also lead to hydrophobic hydrogen terminated Si

surfaces once the surface oxide is removed. This leads one to the speculation that HF and OH<sup>-</sup> chemistry may be similarly removing Si atoms bonded to electronegative elements by back-bond attack of the polarized Si-Si bond. It is also interesting to note that HF and OH<sup>-</sup> in solution may have similarities in their reaction pathways at the surface. Pursuing this idea is clearly a direction for future research.

### 3.2 Structure and Morphology

**Techniques.** The atomic structure of silicon surfaces can only be inferred indirectly using diffraction, imaging and vibrational techniques. The information is therefore subject to the limitations of each technique. The aim of this section is to summarize briefly the information obtainable from each technique and their respective limitations.

**Diffraction Techniques: LEED, RHEED and X-Rays.** Low Energy Electron Diffraction (LEED) and Reflection High Energy Electron Diffraction (RHEED) have been used extensively to study the nature of the long range order of crystalline surfaces. With normal incidence LEED and grazing incidence RHEED, the electrons penetrate 2 - 5 layers into the substrate depending on the electron energy. The diffraction pattern is therefore dominated by the bulk, i.e., most of the diffracted intensity is concentrated into the bulk diffraction beams (integral order beams). When the surface is reconstructed or when regular arrays of steps are present on the surface, additional diffraction spots are present in the pattern, reflecting the extra periodicity. Using electron optics, these additional spots can be Fourier transformed to give real space images of the reconstructed or stepped areas (Low Energy Electron Microscopy) (67). This technique is particularly useful when the surfaces are macroscopically inhomogeneous but locally ordered.

LEED and RHEED give much more limited information when the surfaces are disordered on an atomic scale, particularly if the surface atoms are in a bulk-like position (i.e., are not reconstructed). The diffraction pattern is then due to the bulk order only. The surface atoms modulate the diffracted intensity and contribute to the diffuse background. Quantification of this background is difficult and is meaningful only in a statistical framework. Therefore, the observation of a 1x1 LEED or RHEED pattern does not imply the existence of an atomically flat, unreconstructed surface, but merely the *lack* of an ordered, reconstructed surface.

When surface contamination is eliminated and extraneous scattering is low, quantitative information on the surface morphology can be obtained using LEED spot profile analysis (68). This technique, based on the measurement of the LEED spot profile as a function of electron energy,

gives a quantitative measure of the step density, and therefore of the surface roughness.

Grazing Incidence x-ray diffraction is a particularly useful diffraction method because there is no requirement for the experiments to be performed under vacuum conditions. At the same time the penetrating nature of x-rays renders the technique the least surface sensitive but makes it possible to probe buried interfaces. Another advantage of x-rays, particularly those produced by electron storage rings at facilities like the National Synchrotron Light Source (NSLS) at Brookhaven, is their very high resolution. The typical resolution function of a 3-axis diffractometer fills only  $5 \times 10^{-10}$  of the Brillouin zone of Si. Such a resolution is necessary because the bulk diffraction is localized in point-like Bragg peaks that are smaller than this resolution element. Point defects and bulk thermal diffuse scattering (TDS) are diffuse in all reciprocal space directions. In contrast, surfaces and interfaces, by virtue of their 2-dimensional translational symmetry, give rise to rod-like lines of scattering (69). Therefore, 3-D Bragg peaks can be filtered out by avoidance and diffuse scattering by background subtraction. The remaining problem is to distinguish the buried interface from the surface through which it is measured. Typically, what is measured is the intensity profile of one of these surface-symmetry-sensitive rods (70). This can then be fit to specific models of statistical disorder that describe the roughness on an atomic level, involving a distribution of occupancy in each layer Si in the region of the interface. As a result, specific information can be obtained on the structure of chemically prepared surfaces as well as that of the Si/SiO<sub>2</sub> interface.

**Imaging Techniques: STM, AFM and TEM.** Unlike diffraction methods, Scanning Tunneling Microscopy (STM) provides images of surfaces with atomic resolution in real space. The microscope produces images by bringing a conducting probe (the tip) up to the sample surface until the separation distance is small enough ( $<10 \text{ \AA}$ ) that the electron tunneling probability is appreciable ( $>10^{-4}$ ). At this point, a measurable current flow may be induced by applying a small bias voltage ( $1 \text{ mV} \rightarrow 4 \text{ V}$ ) between the tip and sample. A feedback system regulates the tunneling current by varying the tip height to maintain a constant *tunneling probability* as the tip is rastered parallel to the average surface plane. Under these bias conditions, the transiting electrons do not follow classical trajectories, but instead obey paths dictated by the laws of quantum mechanics. The STM owes its vertical resolution ( $\sim 0.1 \text{ \AA}$ ) to the fact that the tunneling probability increases by an order of magnitude for each angstrom increase in tip-sample separation, and its lateral resolution ( $\sim 2 \text{ \AA}$ ) to the atomic nature of the probe tip and sample. This allows unusual features in the electronic

density of state of the tip to influence the tunneling images under some conditions (71). Furthermore, the appearance and even symmetry of the images are dependent on the polarity and magnitude of the bias voltage (72), especially for highly reconstructed semiconductor surfaces, such as those of silicon and germanium. One must therefore bear in mind that the STM produces images of integrated electronic density of states, *not atom core positions*.

The Atomic Force Microscope (AFM) is a related scanning probe microscope which generates real-space images in a similar fashion to the STM, namely by sensing the attractive/repulsive force between a probe tip and the sample surface as the distance between the two is reduced. For this reason, it holds much promise in atom-by-atom imaging of *insulating* materials. Currently, atomic resolution has only been achieved when the AFM is operated in its repulsive mode (thus with the tip "touching" the sample), raising the question of possible damage. The best resolution obtained in the noncontact attractive mode has been  $\sim 100 \text{ \AA}$ . Stable operation in the attractive mode has been limited by the difficulty in producing a reliable mechanical system with a large enough dynamic range.

Transmission Electron Microscopy (TEM) uses high energy (100 keV) electron scattering to image interfaces and bulk materials. Both plan-view and cross-sectional TEM gives useful structural information about surfaces and interfaces. Like x-ray diffraction, the penetration of the probe is relatively deep ( $\sim 500 \text{ \AA}$ ), which makes it one of the techniques that can be applied to buried interfaces.

**Vibrational Spectroscopies: Inelastic He Scattering, EELS and IRAS.** Vibrational spectroscopies are the least obvious structural techniques. Yet, detailed information about local and extended structures is contained in the vibrational spectra of clean surfaces (substrate phonons) and of adsorbate layers (overlayer modes). This is particularly true when the overlayer contains light elements (e.g., H), because the associated vibrational modes are found at a high frequency and are well separated from the substrate phonons.

Inelastic He atom scattering is a high resolution vibrational spectroscopy, best suited for the study of low frequency ( $< 500 \text{ cm}^{-1}$ ) phonons on *well-ordered* crystalline surfaces (3). A monoenergetic beam of thermal energy ( $\sim 0.04 \text{ eV}$ ) He atoms is completely reflected by the surface (no penetration into the bulk). The reflected beam is analyzed by use of time-of-flight techniques yielding high spectral resolution ( $\sim 0.1 \text{ cm}^{-1}$ ). The large mass of the He atom, relative to that of an electron, makes it possible to impart a large momentum together with energy to the surface phonons. This technique can thus investigate the *dispersion* of surface phonons over

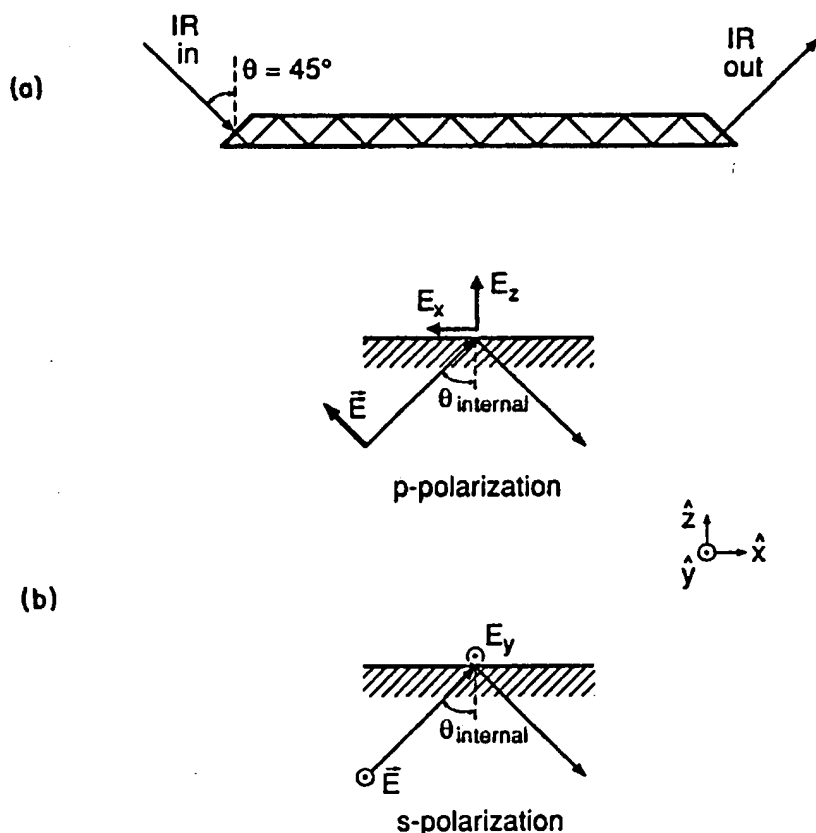
the whole surface Brillouin zone (SBZ) ( $\sim \text{\AA}^{-1}$ ). The dispersion results from surface interactions within a well ordered domain and is, therefore, a sensitive measure of surface order. The technique is restricted to low frequencies ( $< 500 \text{ cm}^{-1}$ ) because the turn around time of He atoms is slow (10 fs) at thermal energies. Increasing the He atom energy shortens the turn around time, but greatly complicates the spectrum with multiphonon effects.

Electron Energy Loss Spectroscopy (EELS) and Infrared Absorption Spectroscopy (IRAS) are very useful techniques to study the microscopic structural arrangement of H-terminated silicon surfaces because they can resolve different hydride phases: monohydrides (relaxed and strained), dihydrides, and trihydrides. In studies of adsorbates with vibrational EELS, 2 - 10 eV electrons are incident on the surface; the reflected electrons (0.1 to 1% of the incident beam) are collected and their energy is analyzed using electrostatic analyzers. A small fraction of the reflected electrons lose a quantum of energy by exciting surface vibrations, through either a long-range interaction (dipole scattering) or a short-range interaction (impact scattering). Dipole scattering is observed only in the specularly reflected direction. For dipole scattering, the spectrum is dominated by the components of vibration perpendicular to the surface (74), just as is the case for optical *external* reflection spectroscopy (75). Indeed, the ratio of the dipole scattering cross-sections of parallel to perpendicular vibrations is proportional to  $n^4$ , where  $n_{\text{Si}} = 3.4$  is the refractive index of silicon. For impact scattering, the cross-section has a more complex dependence on the mode polarization and has also a more complex angular dependence that can sometimes be used to give symmetry information about the vibrational modes.

An important attribute of EELS is its large spectral range (0.01 - 2 eV) for vibrational studies. This range includes the frequencies of the silicon surface phonons and of all the silicon-hydrogen vibrations. Furthermore, the intensity of the specular beam (and to a lesser extent, the spectral resolution) depend on the surface morphology and can therefore be used to characterize surface roughness. Its main drawback is the limited resolution ( $\sim 20 \text{ cm}^{-1}$ , although recent advances have made it possible to increase it by a factor of three) (76). Both inelastic He atom scattering and EELS require the introduction of the samples into vacuum, which is a disadvantage for wet-chemically prepared silicon samples.

Infrared absorption spectroscopy is especially sensitive when a multiple internal reflection (MIR) geometry can be used (see Fig. 14). For silicon, the sensitivity to parallel and perpendicular components of the

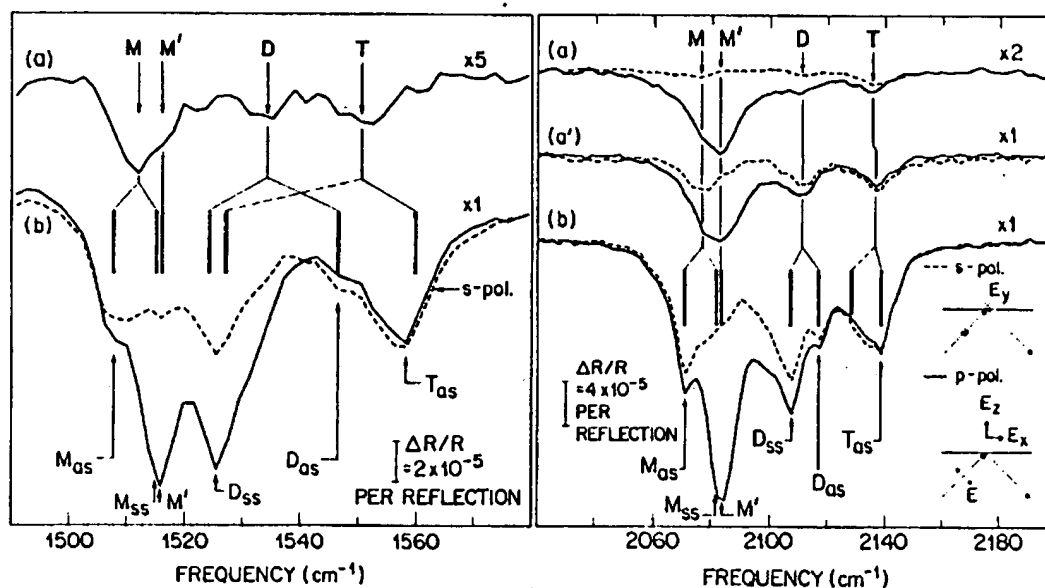
adsorbate vibrations (i.e., above the silicon surface plane) is nearly the same (within 20% for  $\theta_{\text{internal}} = 45^\circ$ ), so that the orientation of *ordered* surface dipoles can be determined, in principle, by use of polarized radiation (see Fig. 14). The accuracy of such orientation determination depends on the precision available in measuring the electronic screening involved in the dynamic interaction between the adsorbates (77). For disordered surfaces, the IR absorption spectra are useful to quantify the *average* orientation of the surface dipoles, and thereby to learn something about the surface disorder and roughness.



**Figure 14.** (a) Side view of a silicon crystal used for multiple internal reflection experiments. Typical dimensions are 3.8 cm length, 2 cm width and 0.05 cm thickness. The short sides are beveled at  $45^\circ$  to allow the IR beam to enter and exit as shown. The total number of reflections in this example is 75. (b) Schematic drawing of the electric fields present on the vacuum side of silicon surface for p-polarization and s-polarization, respectively.

When the H-terminated silicon surfaces are homogeneous, the high resolution ( $\leq 0.1 \text{ cm}^{-1}$ ) of the IR technique gives a wealth of information. For instance, different hydride species can be identified based on the Si-H stretch spectra alone. Experimentally, the mode assignments are simpli-

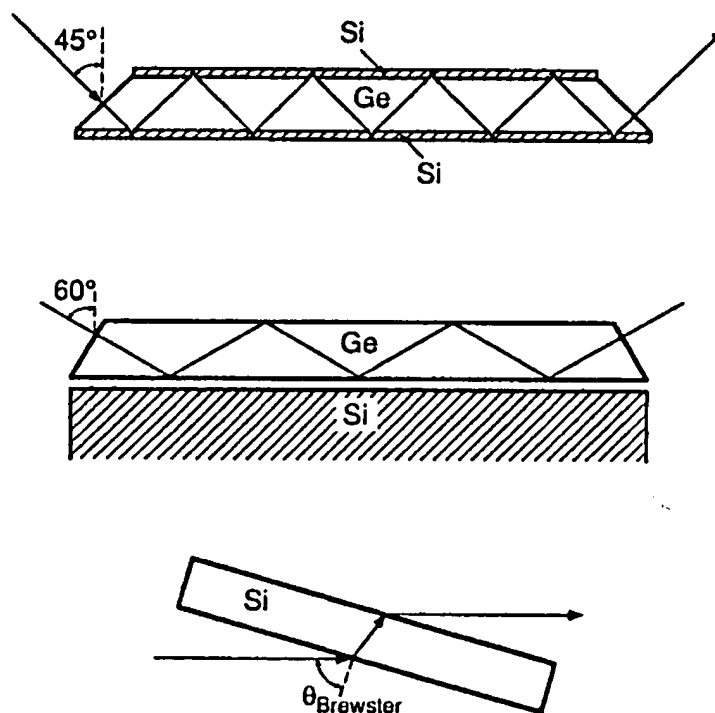
fied by doing isotopic mixture experiments. In this manner, H-stretches can be studied in the dilute limit, where coupling to near neighbor atoms is suppressed due to the mass difference between H and D. The thus obtained "isolated spectra" are simplified (no dynamical splittings), and are only composed of bands associated with fundamentally different species. As can be seen in Fig. 15, the isolated spectra (a) are simpler than the isotopically pure spectra (b). The three fundamental bands are associated with mono-, di-, and tri-hydride species (59). Unambiguous assignments are based on state-of-the-art first principles cluster calculations of force constants and normal frequencies of vibration. The results of such calculations for the isolated frequencies along with their associated splittings are shown schematically in Fig. 15 as vertical bars. The band positions of the isolated frequencies of the mono-, di-, and tri-hydrides and the mono-, di-, and tri-deuterides are in good agreement with the measured values depicted in Fig. 15. Furthermore, the splittings evaluated from the measured isolated frequencies are in excellent agreement with the measured values for both the hydride and the deuteride stretches (59).



**Figure 15.** Polarized IR absorption spectra of the Si-D stretch vibrations (left panel) and Si-H stretch vibrations (right panel) for various isotopic concentrations after etching of a Si(111) sample in dilute HF/DF.

In the left panel, (a) corresponds to 7% D and 93% H on the surface and (b) to 95% D and 5% H. The observed isolated frequencies are  $M = 1512 \text{ cm}^{-1}$ ,  $D = 1533.5 \text{ cm}^{-1}$ , and  $T = 1550 \text{ cm}^{-1}$ . In the right panel, (a) corresponds to 10% H and 90% D, (a') to 25% H and 75% D, and (b) to 100% H. The observed isolated frequencies are  $M = 2077 \text{ cm}^{-1}$ ,  $D = 2111 \text{ cm}^{-1}$ , and  $T = 2137 \text{ cm}^{-1}$ . In both cases, the thick vertical bars represent the calculated coupled mode splittings from the measured isolated frequencies, as shown in the previous figure. (From Ref. 58.)

The transmission cut-off at low frequencies is the main limitation of the multiple internal reflection (MIR) geometry. It is particularly severe for silicon, which is opaque below  $1500\text{ cm}^{-1}$  due to multiphonon absorption (78). To study modes below this frequency, different schemes can be used (Fig. 16). If silicon can be grown epitaxially on germanium, then the MIR geometry can still be used with the germanium as the main substrate material (transparent above  $650\text{ cm}^{-1}$ ), as shown in Fig. 16 (top). Alternatively, the silicon sample can be pressed against a germanium MIR plate (see Fig. 16, middle), giving good sensitivity to modes *normal* to the surface (79)–(81). Otherwise, a transmission or external reflection geometry can be utilized to minimize the substrate absorption. In general, the transmission geometry (e.g., at the Brewster angle shown in Fig. 16, bottom) gives a better sensitivity than the reflection geometry (82).



**Figure 16.** Various configurations for studying surface vibrations in a range of substrate absorption.

**Results.** This section starts with the effects of aqueous HF (concentrated and dilute HF solutions) on the surface morphology of Si(100) and Si(111). We then examine separately the etching of Si(100) and Si(111) in buffered HF solutions. Throughout these sections, the nature of the starting



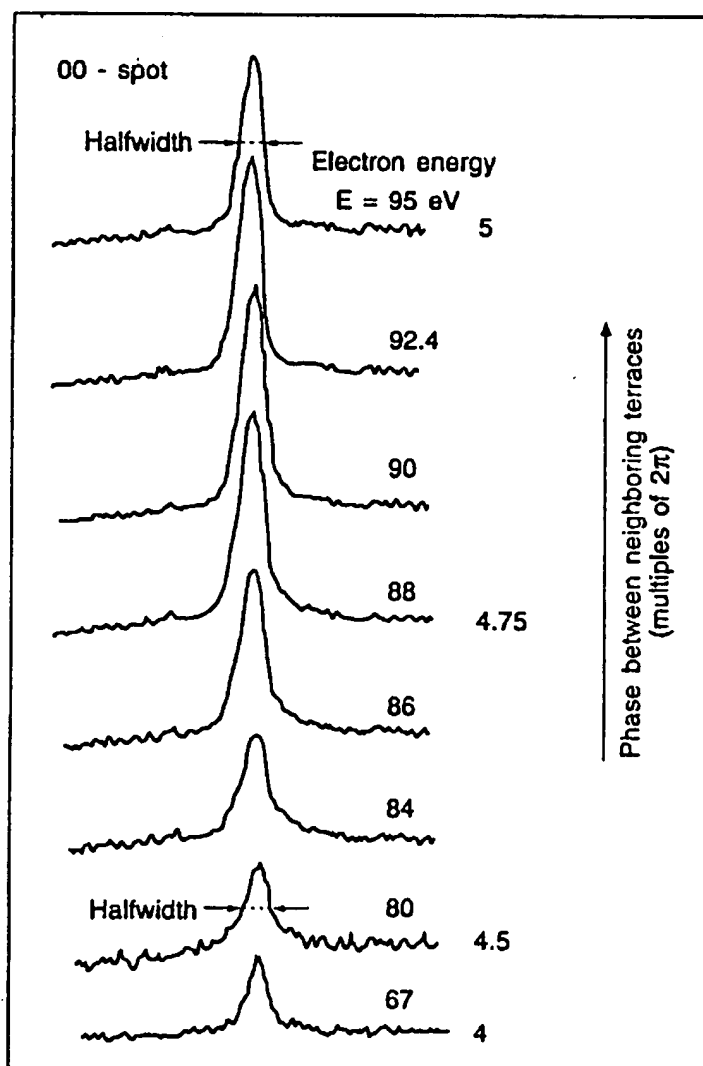
Si/SiO<sub>2</sub> interfaces and the role of water (e.g., rinsing) in the etching process are also considered since they are relevant to the final surface structure

***Si(100) and Si(111) Etched in Aqueous HF Solutions.*** The first information available on the morphology of H-terminated Si(100) and Si(111) was the study by Hahn and Henzler (1984) (3). Their goal was to use LEED for investigating the Si/SiO<sub>2</sub> interface morphology as a function of oxidation conditions and polishing methods. As with most surface analysis techniques, LEED requires SiO<sub>2</sub> film removal prior to the measurement. This was achieved by dissolving the oxide layer in concentrated HF followed by rapid load-locking into the analysis chamber. In this manner, the densities of step-atoms could be studied as a function of oxidation conditions. An example of how the analyses were performed is found in Hahn (1986) (83), where LEED spot-profile-analysis was used to study the atomic structure of chemo-mechanically polished Si(111) wafers. The original data, shown in Fig. 17, demonstrated that chemo-mechanically polished Si(111) etched in concentrated HF is step-free over 100 Å distances, on the average. In such an experiment, the electron wavelength is varied by varying the electron energy, leading to in-phase and out-of-phase scattering conditions from one atomic layer to another. The lack of broadening as a function of the electron wavelength shown in Fig. 17 indicates that the width is instrumentally limited and gives a lower limit for the average length of the terrace of 100 Å.

Next, Grundner and Schulz (1988) (55) used the vibrational frequency information from their electron energy loss spectra (EELS) on HF-treated Si(111) and Si(100) to investigate the nature of the H-termination. The main conclusion of this study was that Si(100) was dihydride terminated and Si(111) was monohydride terminated. Conclusive evidence for the dihydride species is the presence of a loss peak at 900 cm<sup>-1</sup>, corresponding to the SiH<sub>2</sub> scissor mode. The EEL spectrum shown in Fig. 10 (top) for Si(100) is characterized by a strong loss peak at 900 cm<sup>-1</sup> and compares well to spectra obtained in UHV upon atomic H dosing of clean Si(100) (84). This finding and the observation of a 1x1 LEED pattern (21) led these authors to the conclusion that a uniform dihydride phase had been obtained. For HF-etched Si(111) surfaces, the strong Si-H stretch loss at 2080 cm<sup>-1</sup> in Fig. 10 (bottom), together with the "good quality" 1x1 LEED pattern (21), led them to conclude that the surface was ideally monohydride-terminated. A weak loss at 900 cm<sup>-1</sup> was attributed to dihydride at steps.

High resolution infrared reflection absorption spectroscopy (IRRAS) is a powerful technique that provides detailed information not available from EELS. Polarized spectra, taken by multiple internal reflection (MIR), are

particularly useful to elucidate the surface structure of H-terminated silicon (see Sec. 3.2, Vibrational Spectroscopies). Contrary to the conclusions drawn from EELS, the infrared studies indicate that both Si(100) and Si(111) surfaces are atomically rough after similar etching treatments.



**Figure 17.** LEED spot profiles of Si(111) polished wafer after HF treatment. (From Ref. 83.)

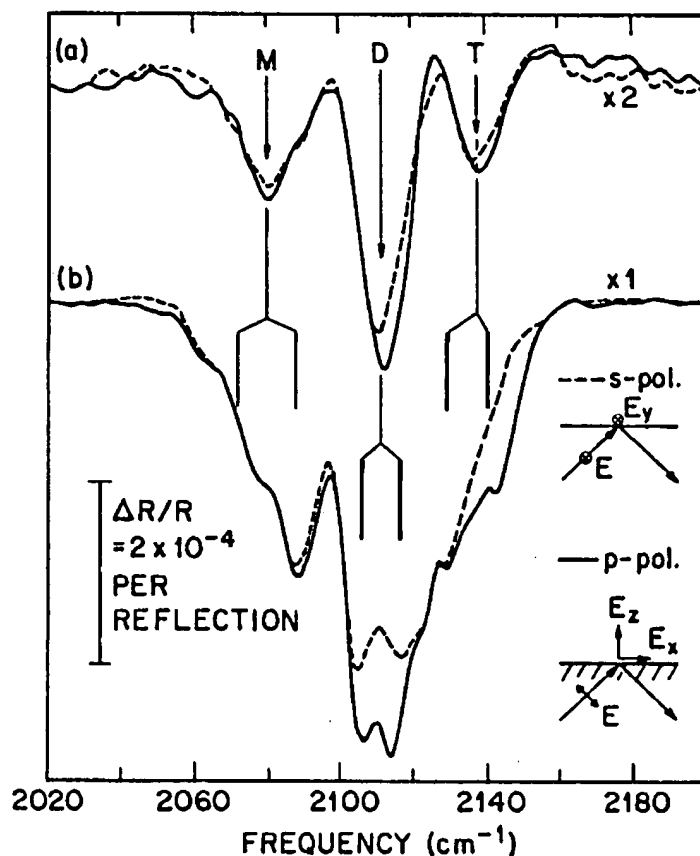
The roughness is evident from the polarized IR absorption spectra shown in Figs. 18 and 15 for Si(100) and Si(111) respectively. The complexity of the hydrogen stretch spectra is clearly observed for both the Si(100) and Si(111) surfaces. An *ideally terminated* Si(100) surface would be characterized by two modes, the symmetric and anti-symmetric dihydride

stretch. Furthermore, the symmetric stretch should be polarized normal to the surface and the anti-symmetric stretch should be parallel to the surface, contrary to what is experimentally observed in Fig. 18. Similarly, an ideally terminated Si(111) would be characterized by a single monohydride stretch mode polarized normal to the surface but is clearly not observed in Fig. 15. Although these surfaces are not ideally terminated, structural information can still be extracted by providing complete assignments of the observed bands. As pointed out in Sec. 3.2 (Vibrational Spectroscopies), the mode assignments of the various hydride species can be performed by using isotopic substitution experiments combined with force constant/normal mode analyses on model compounds (59). The silicon-hydrogen stretch spectra in Fig. 18a and Fig. 15 (a and a', right frame) are simpler because the major species is deuterium, i.e., the hydrogen atoms are isolated from each other. The three main bands in the isolated spectra are assigned to the monohydrides (coupled M or not coupled M'), to dihydrides (D) and trihydrides (T). The corresponding spectrum for the silicon-deuterium stretch (a) for the isolated deuterium, and the coupled spectra (b), shown in Fig. 15 (left frame), confirm these assignments. The solid vertical bars in Figs. 15 and 18 correspond to the theoretical predictions for the splittings associated with each hydride structure, starting from the measured value of the isolated frequency (58)(59). With these mode assignments the structure of these H-terminated surfaces can be obtained.

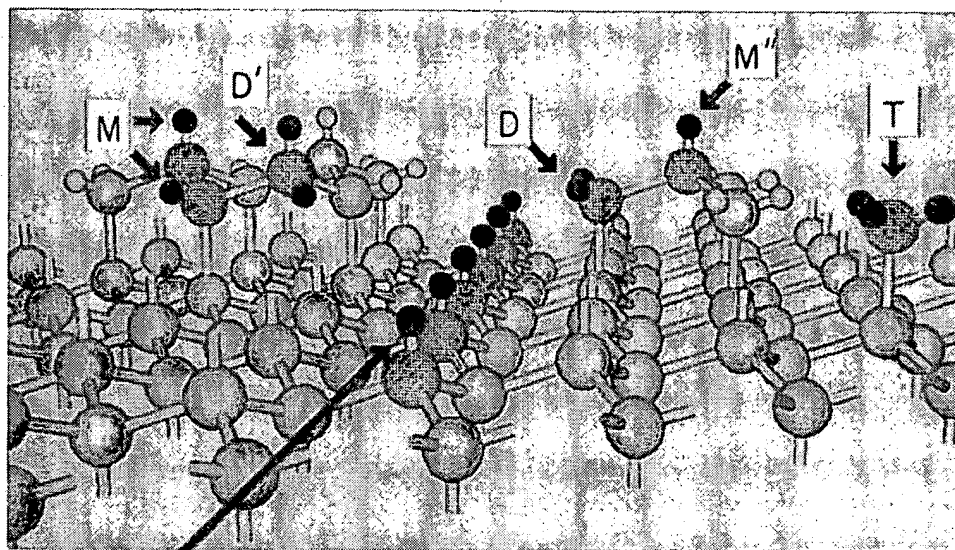
The isolated spectra in Fig. 18a show that dihydrides are the dominant species on the Si(100) surface, an observation consistent with the EELS studies. It is important, however, to point out that the dihydride observed in Fig. 18 is not the same as the dihydride observed on atomically flat Si(100) prepared in UHV by exposure to atomic H. The latter dihydride has its axis normal to the surface and is surrounded by strained monohydride units (85). The exact morphology of these chemically prepared Si(100) surfaces, however, cannot be inferred accurately from the IR spectra alone. The relative concentrations of mono-, di-, and tri-hydrides give qualitative information of the average surface morphology and are only useful for comparison.

For Si(111), the spectra in Fig. 15a are dominated by monohydride stretches, in agreement with the EELS data. In this case, part of the monohydride spectrum (M') is found to be polarized normal to the surface and can be associated with ideal termination (monohydride on a Si(111) terrace) (77)(86). Having identified the M' mode, the relative intensities of M, D, and T modes can be used to deduce the average surface structure, schematically represented in Fig. 19. In this figure, M terminates the side

of adstructures and T terminates the (111) terraces. There are two types of uncoupled monohydrides ( $M'$ ) and the ideal monohydride, ( $M''$ ) and two types of dihydrides (D and  $D'$ ).  $M''$  has not been measured separately, either because its frequency is too close to that of the  $M'$  and/or because its concentration is too low to be detectable. These data do show that only a quarter of the surface is covered with  $M'$ . Step edge monohydrides (coupled monohydride, M) comprise another quarter of the surface. Together, they make up approximately half of the surface hydrides leading to the strong monohydride EELS signature. Although, there appears to be an apparent contradiction to the EELS results, where no dihydrides were observed, EELS suffers from problems with interpretation depending on whether the scattering mechanism is believed to be dipolar (87)(88) or non-dipolar (62). The IR spectra give quantitative information of the dihydride stretch.



**Figure 18.** Polarized IR absorption spectra of the Si-H stretch vibrations for two isotopic concentrations after etching of a Si(100) sample in dilute HF/DF. (a) corresponds to 20% H and 80% D, and (b) to 100% H. The thick vertical bars represent the calculated coupled mode splittings from the measured isolated frequencies (labeled M, D and T). (From Ref. 59.)



### IDEAL (111) TERMINATION M'

**Figure 19.** Schematic representation of possible surface structures on the Si(111) surface with their associated hydrogen termination. The ideal monohydride and trihydride termination are possible for an atomically flat (111) plane. The "horizontal" dihydride (D) terminates the corner of a small adstructure where an isolated monohydride (M'') may exist. Both the "vertical" dihydride (D') and coupled monohydride (M) can terminate larger adstructures of the type shown here. These are all the possible structures that do not involve surface *reconstruction*. (From Ref. 58.)

The "horizontal" dihydride (D in Fig. 19.) has been observed on the rough Si(111) at a frequency slightly shifted from that of the relaxed dihydride on Si(100) (85). The second type of dihydride (D'), in a plane perpendicular to the surface, has been extensively studied in the context of vicinal surfaces (miscut toward the  $\langle \bar{1}12 \rangle$ ) (89). Notice that in Fig. 19 many dangling bonds have been left unterminated for clarity. HF etched surfaces, however, are completely hydrogen terminated. This implies that there would be a strong interaction between the "vertical" dihydride (D') and the terrace monohydride directly beneath it. This steric interaction leads to the appearance of three stretch modes, at 2094, 2101, and 2135  $\text{cm}^{-1}$ , (89) instead of only two in the 2110  $\text{cm}^{-1}$  region for the unconstrained dihydride.

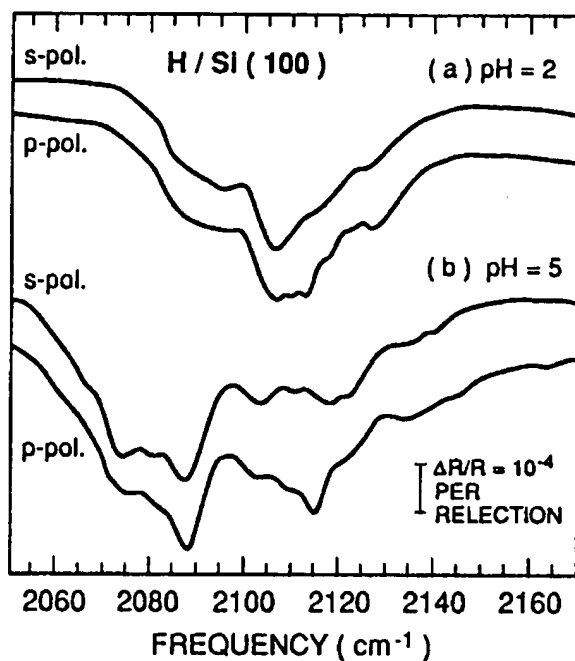
The observation of trihydride on the Si(111) surfaces is both interesting and controversial. It is clear from the isolated spectra of Fig. 15a that trihydride is present. Its concentration, however, is relatively low. It is now understood that a fraction of the strength of the mode labeled  $T_{as}$  at 2139

$\text{cm}^{-1}$  in Fig.15b arises from the  $2135\text{ cm}^{-1}$  mode of the vertical dihydride ( $\text{D}'$ ). Recent STM images of Si(111) etched in 1% HF solutions (90) have shown a pattern more consistent with the presence of large regions terminated by trihydrides than of the small adstructures described above. This conclusion is based on the observation of threefold symmetry and  $2.2\text{ \AA}$  periodicity in the STM images, which is inconsistent with a Si lattice spacing. The most likely close-packed trihydride arrangement involves a rotation of neighboring trihydrides leading to an average H-H distance of  $\sim 2.2\text{ \AA}$  (91). If the trihydride concentration is larger than 10% of a monolayer, these STM results are not consistent with the IR absorption spectra (59)(66) which indicate that mono- and di-hydrides are more numerous than trihydrides on Si(111) surfaces etched in dilute HF. The IRRA spectra also fail to show the mode at  $2154\text{ cm}^{-1}$  associated with a uniform trihydride phase, observed upon adsorption and decomposition of di-silane (92). In addition, previous STM studies of Si(111) surface etching in dilute HF, while showing the surface roughness predicted by the IR data, did not show any evidence for a uniform trihydride phase (93). In view of these contradictions, the nature of the trihydride must be clarified in future work.

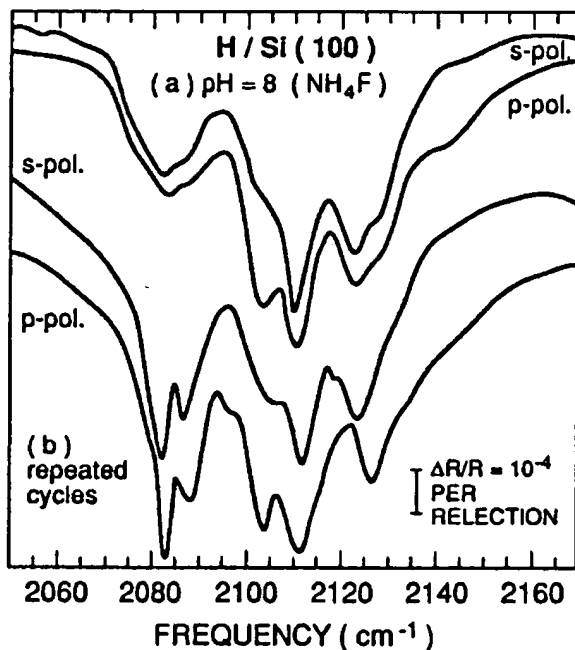
The main conclusion of the results presented above is that etching in dilute HF leads to atomically rough surfaces. Mono-, di-, and tri-hydrides coexist on both Si(100) and Si(111) surfaces. STM images of Si(111) (93) show structures of  $10 - 20\text{ \AA}$  diameter and  $3\text{ \AA}$  in height, accounting for about 50% of the surface, consistent with the IR data.

***Si(100) Etched in Buffered HF Solutions.*** Buffered HF is composed of various mixtures of 50 wt% HF in  $\text{H}_2\text{O}$  and 40 wt%  $\text{NH}_4\text{F}$  in  $\text{H}_2\text{O}$ . A common mixture used in the industry is 7:1 buffered HF, which has a pH of 4.5 and is composed of 7 volumes of  $\text{NH}_4\text{F}$  and 1 volume of HF. The main difference between aqueous HF and buffered HF is the solution pH, which is the object of the following discussion.

Raising the pH of the HF solution increases the etch rate of the H-terminated silicon surfaces. Figs. 20 and 21 clearly show that the morphology of chemically prepared Si(100) surfaces changes as the pH of the etching solution varies from 2 to 8. For a pH of 2 (Fig. 20a), the IR absorption spectra are dominated by dihydrides. In buffered HF (pH  $\sim 5$ ), the spectrum sharpens and is dominated by coupled monohydrides (Fig. 20b). For higher pH's, the etching proceeds quickly, as evidenced by the gas bubbles forming at the sample surface. After etching in an ammonium fluoride solution (pH = 7.8), the dihydride contribution is again dominant (Fig.21a).



**Figure 20.** Polarized IR absorption spectra of Si(100) surfaces etched in: (a) dilute HF (1%, pH = 2) and (b) buffered HF (pH = 5). The chemically oxidized surface is used as a reference and the spectral resolution is  $1 \text{ cm}^{-1}$ . (From Ref. 62.)



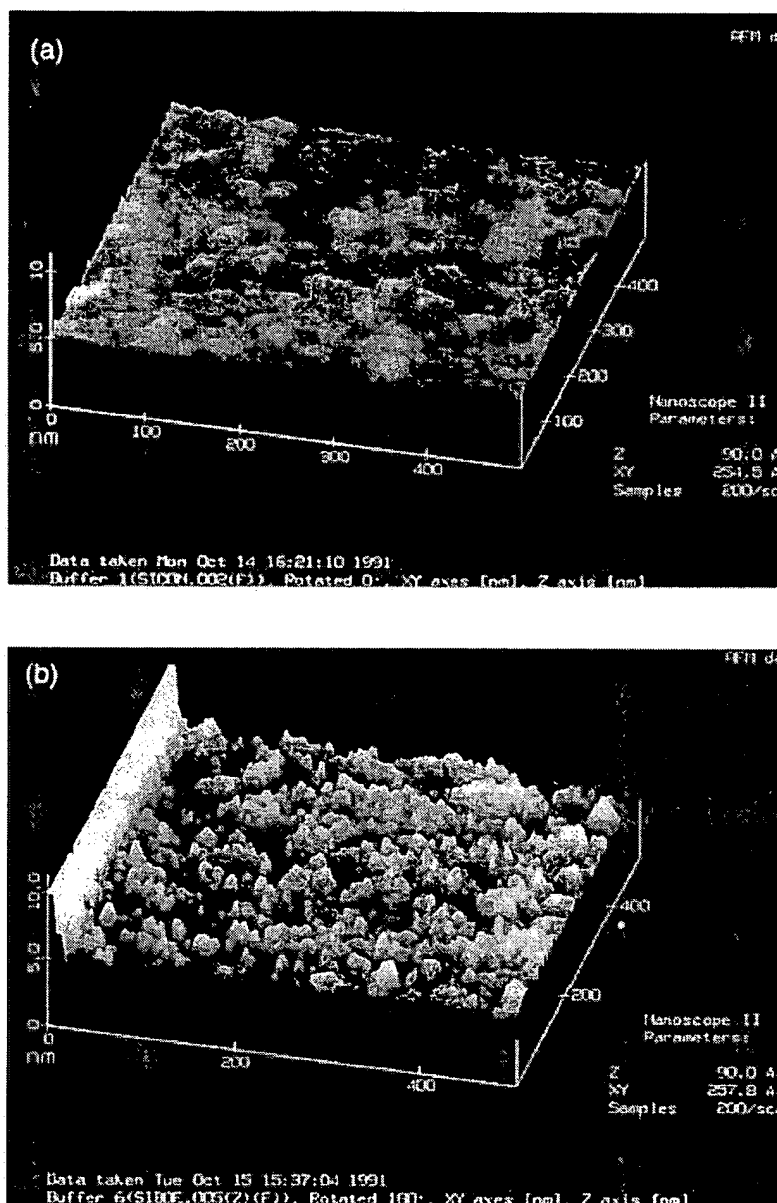
**Figure 21.** Polarized IR absorption spectra of Si(100) surface etched in a 40%  $\text{NH}_4\text{F}$  solution (pH = 7.8) once (a) and after repeated cycles of etching in a 40%  $\text{NH}_4\text{F}$  solution, chemical reoxidation in  $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$  (4:1:1) at  $80^\circ\text{C}$ , and a final etching in  $\text{NH}_4\text{F}$  (b). (From Ref. 62.)

The dihydride dominated spectra shown in Fig. 20a ( $\text{pH} = 2$ ) are the result of a treatment in dilute HF, and represent a surface which is rough on an atomic scale, as previously discussed. The dominance of the monohydride modes in Fig. 20b suggests the formation of microfacets on the Si(100) surface (62)(65). At high pH (Fig. 21a), although the spectra revert back to being dominated by the dihydride stretch, the polarization of this mode is quite different from the  $\text{pH} = 2$  spectra. In this case, the symmetric stretch ( $2105 \text{ cm}^{-1}$ ) is polarized normal to the surface and the anti-symmetric stretch ( $2112 \text{ cm}^{-1}$ ) is polarized parallel to the surface. Although, these polarizations would be correct for terrace dihydride, for the reasons given above, these surfaces are not believed to be atomically flat because of the existence of spectral contributions from mono- and tri-hydride that are still very strong. Furthermore, the monohydride spectrum is now centered around  $2085 \text{ cm}^{-1}$ , indicating the growth of (111) facets.

After several etching cycles, Fig. 21b shows that two sharper modes are resolved at  $2084$  and  $2088 \text{ cm}^{-1}$ . The first is assigned to the Si-H stretch of the ideal Si(111) monohydride, confirming that (111) facets develop in solutions of high pH. The second is probably associated with the symmetric stretch of coupled monohydrides; the asymmetric stretch mode is more highly screened and therefore not observed. Both types of monohydrides have symmetric stretches pointing away from the normal of the macroscopic surface plane and are therefore unscreened. In contrast, the dihydride modes in Fig. 21 are characteristic of dihydrides with their axis pointing along the surface normal. The simplest atomic arrangement consistent with these observations is a distribution of tent-like structures with a row of dihydrides at the roof top, (111) facets terminated with ideal monohydride on the sides and coupled monohydride at the periphery of the facets. Since the facets are small, the concentration of coupled monohydrides is as high as that of ideal monohydrides.

The use of buffered HF may be ill-advised in attempting to prepare atomically flat (100) surfaces, since (111) facets develop upon etching. Increased surface roughness has been directly observed after buffered HF etching (24)(28). As shown in Fig. 22, a control wafer is relatively smooth with  $\sim 2 \text{ \AA}$  rms roughness, whereas, a wafer treated in buffered HF is characterized by  $\sim 5 \text{ \AA}$  rms roughness. In attempting to smooth Si(100) surfaces, one might use thermal oxidation that is known to result in high-quality Si/SiO<sub>2</sub> interfaces. In such an experiment, a  $1000 \text{ \AA}$  thick dry O<sub>2</sub> oxide was grown at  $1000^\circ\text{C}$  and post-annealed in Ar at this temperature for 30 min. The oxide was then removed with concentrated HF. The complex spectra obtained give conclusive evidence that atomically inhomogeneous surfaces again result.





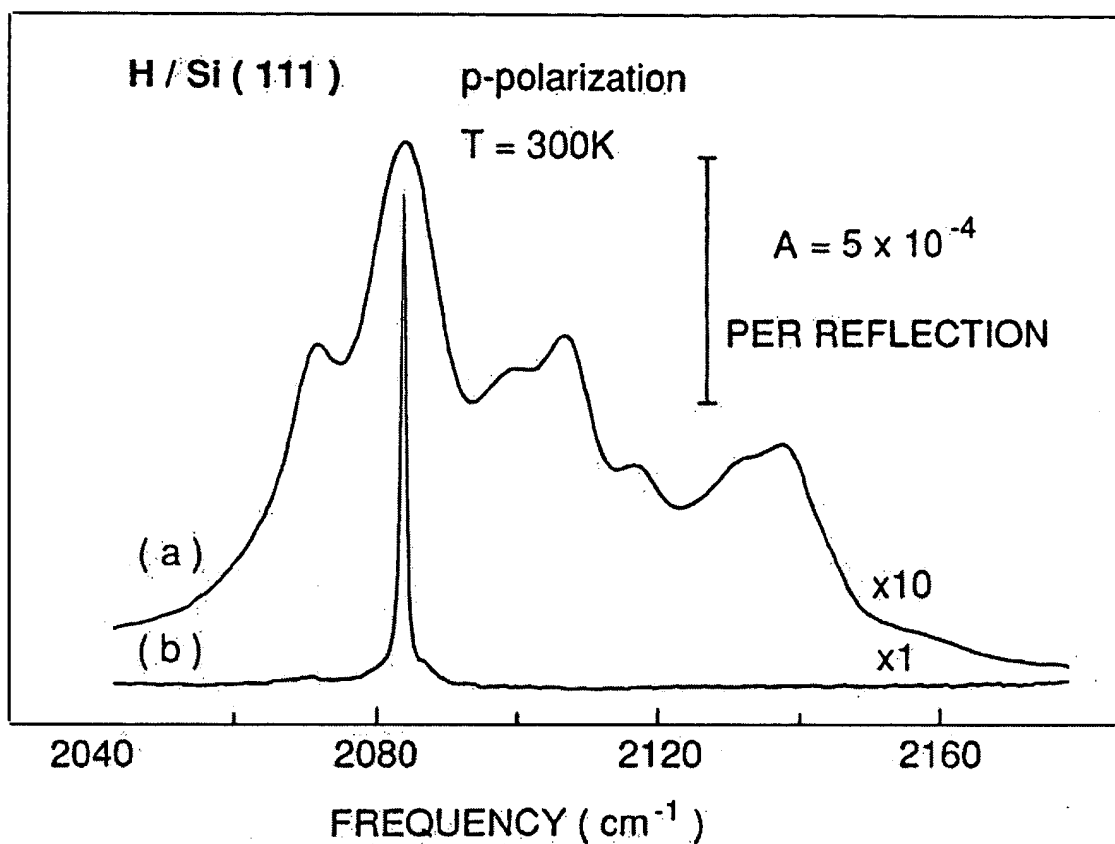
**Figure 22.** Atomic force microscope images of (a) a chemo-mechanically polished Si(100) control wafer ( $\sim 2$  Å rms) and (b) a Si(100) wafer etched in 7:1 buffered HF solution for 10 min ( $\sim 5$  Å rms).

In summary, Si(100) surfaces are microscopically rough when treated in either dilute or concentrated HF. These surfaces are macroscopically roughened by buffered HF solutions due to (111) facet formation. To date, little is known about the nature of such surfaces. The potential impact on the quality of subsequent interfaces formed after further processing will motivate future work in this area.

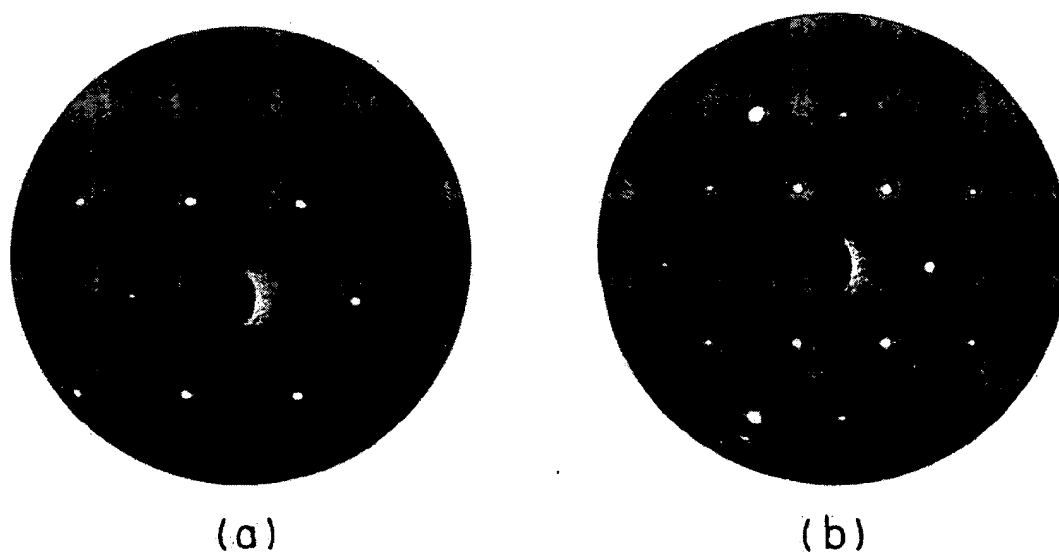
***Si(111) Etched in Buffered HF Solutions.*** For the Si(111) surfaces, increasing the pH of the solution leads to a *preferential* etching of the H-terminated surfaces, making it possible to flatten the surface on an atomic scale (65). For instance, Fig. 23 shows the difference between a Si(111) surface etched in dilute HF and buffered (pH ~8) HF solutions. Whereas the dilute HF etched surface is atomically rough (Fig. 23a) with all forms of hydrides, the surface etched in a 40 wt%  $\text{NH}_4\text{F}$  solution is characterized by a single sharp absorption line at  $2083.7\text{ cm}^{-1}$ , polarized perpendicular to the surface (Fig. 23b). The obvious implication is that atomically flat surfaces have been obtained with ideal monohydride termination. In the first report, (65) it was noted that the measured linewidth,  $\Delta\nu \sim 0.9\text{ cm}^{-1}$ , was the narrowest line ever measured for a chemisorbed atom or molecule on a surface *at room temperature*. Part of the width, however, could still be due to thermal broadening. A method was therefore devised to introduce the wafers samples into UHV, making it possible to cool them so that the inhomogeneous linewidth could be measured. The data confirmed that most of the linewidth measured at room temperature was thermally induced, due to an harmonic coupling of the Si-H stretch mode to surface silicon phonons (86). At present, the best samples are characterized by an extremely small ( $0.05\text{ cm}^{-1}$ ) inhomogeneous broadening (77)(94). This result indicates a high degree of homogeneity and has motivated thorough characterization by most of the techniques described in Sec. 3.2.

The LEED patterns obtained after careful introduction into UHV show a  $1\times 1$  pattern with resolution limited integral order spots and a background below the detection limit of conventional LEED systems (Fig. 24). This unreconstructed and ideally H-terminated surface is often referred to as the H/Si(111)-(1 $\times$ 1). Quantitative diffraction studies with SPA-LEED and x-ray diffraction are underway that should be particularly useful to characterize the roughness of Si(111) etched at lower pH, using H/Si(111)-(1 $\times$ 1) as a reference.

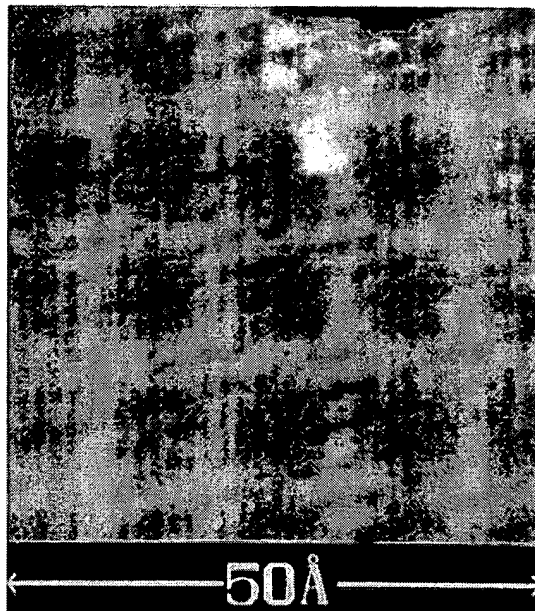
STM images (93)(95) such as the one shown in Fig. 25, have confirmed that the surface is nearly contamination free (<1 ML), atomically flat, and well ordered with  $1\times 1$  ( $3.84\text{ \AA}$ ) periodicity. The electronic structure obtained from (dI/dV) measurements displays no states in the gap, which is expected for a hydrogen-covered surface. Further support for the bulk-like character and the ideal monohydride termination comes from electron-stimulated desorption experiments (96) showing the formation of the  $\pi$ -bonded chains (2 $\times$ 1) reconstruction after the H is desorbed. This surface has also been imaged with an atomic force microscope, confirming the  $1\times 1$  periodicity (97).



**Figure 23.** P-polarized IR absorption spectra of Si(111) after (a) etching in dilute HF (pH = 2), and (b) a 40%  $\text{NH}_4\text{F}$  solution (pH = 7.8). (From Ref. 62.)



**Figure 24.** Photograph of LEED pattern of Si(111) surface after  $\text{NH}_4\text{F}$  treatment: (a) 82 eV and (b) 125 eV. (From Ref. 93.)



**Figure 25.** STM picture of H/Si(111)-(1x1). The vertical grey scale is 0.5 Å. (From Ref. 93.)

An alternate means of characterization is to measure the low frequency surface vibrations (Si phonons) of this surface. Theoretical calculation of the vibrational manifold (98) predict strong dispersions for the modes of this ordered surface. Inelastic helium atom scattering measurements, performed by Doak et al. (1990) (99), show phonon losses up to 30 meV ( $250\text{ cm}^{-1}$ ). Two phonon branches ( $S_8$  and  $S'_8$ ) at 27.4 and 23.7 meV, respectively, are observed to disperse in addition to the Rayleigh wave between 0 and 16.3 meV, consistent with a well-ordered surface. The incoherent elastic scattering and broad inelastic backgrounds are almost two orders of magnitude lower than that measured for H-terminated Si(111) prepared using standard UHV techniques (100). This confirms the perfection of the surface compared to surfaces prepared in UHV.

The EELS studies of the H/Si(111)-(1x1) are similarly characterized by a very high specular beam intensity and a low background (61). Recently, the dispersion of both the silicon phonons and the H vibrations has been measured (62)(101) in good agreement with the calculated curves (98).

High resolution IR absorption spectra recorded at low temperatures ( $<50\text{ K}$ ) have also been used to characterize the extent of the perfect 1x1 domains (77)(94). Below 50 K, the lifetime ( $\sim 0.005\text{ cm}^{-1}$ ) (102) and thermal ( $<0.001\text{ cm}^{-1}$ ) (86) broadenings are negligible compared to the measured

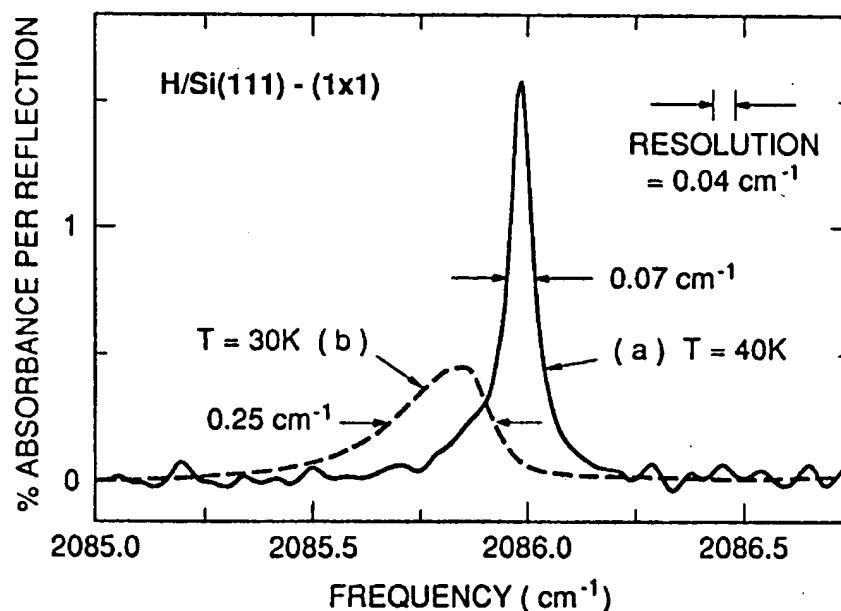
linewidth ( $0.07\text{ cm}^{-1}$ ) (Fig. 26a). After deconvolution of the resolution function ( $0.04\text{ cm}^{-1}$ ), the natural linewidth ( $0.05\text{ cm}^{-1}$ ) and the line shape are obtained and can be related directly to surface inhomogeneities.

In considering the line shapes, Jakob et al. (1991) (77) pointed out that a distribution of point defects leads to a symmetrical broadening (such as Lorentzian or Gaussian), whereas the presence of finite domains leads to an asymmetric broadening. This asymmetry is dominated by effects associated with dipole coupling between the hydrogen atoms. For a finite domain containing  $N$  atoms, there are  $N$  normal modes. The strongest IR active mode is the "in-phase" normal mode. This normal mode is at the highest frequency, and this frequency increases with domain size because Si-H is oriented perpendicular to the surface. A few other normal modes, however, also have a strong enough IR cross section ( $\sim 3 - 5\%$  of the in-phase mode) to be detectable and give a low-frequency tail to the absorption band. Furthermore, the measured absorption associated with a distribution of domain sizes is proportional to  $P(N) \times N$ , where  $P(N)$  is the distribution function (the bigger domains contribute more to the absorption). Therefore, a symmetric distribution of domain sizes leads to an asymmetric absorption line shape, characterized by a low frequency tail for the Si-H system. When both effects are taken into account, the spectra of Fig. 26a can be well fit with  $N = 2 \times 10^4$  Si-H units with a 30% distribution in domain size (77). Recent STM images show that the average linear terrace size is  $500\text{ \AA}$  on flat samples in excellent agreement with the IR absorption line shape analysis ( $\sim 600\text{ \AA}$ ) (103).

The nature and origin of point defects is not completely clear at present; triangular pits, with  $5 - 20\text{ \AA}$  sides and a double layer deep, and "white balls" have been observed with STM (95)(103). These defects are not observed on all samples and could depend on process and materials parameters, such as doping, solution pH, etching rate, sample vicinality, etc.

The sensitivity of the IR absorption technique makes it possible to investigate various preparations of the surface in detail. In particular, the nature of the oxide prior to the HF etching has been found to be important. Fig. 26 shows high-resolution spectra associated with H/Si(111)-(1x1) surfaces prepared in two different ways: (a) by stripping the thick thermal oxide in buffered HF ( $\text{pH} = 5$ ) and directly dipping the H-passivated sample into a 40 wt%  $\text{NH}_4\text{F}$  solution for 4 min, and (b) by reoxidizing chemically (SC-2) and then stripping and re-etching in a 40 wt%  $\text{NH}_4\text{F}$  solution for 6 min. The first absorption line was discussed in detail above. The second spectrum peaks at lower frequency, indicating a smaller average domain size. It is

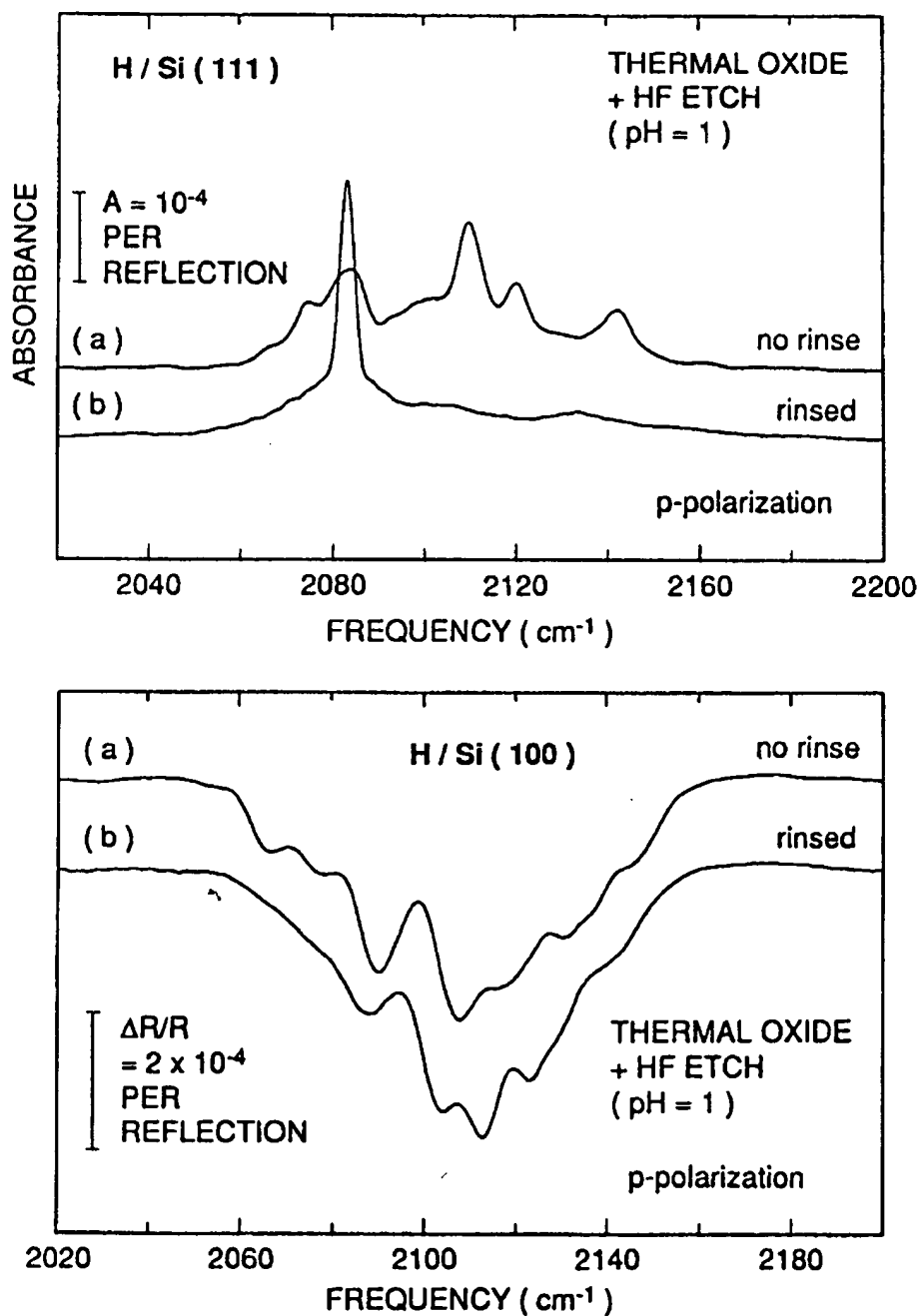
also broader, indicating a larger distribution of domain sizes. Therefore, thermally grown oxides result in a smoother interface than chemically grown oxides.



**Figure 26.** P-polarized IR absorption spectra of H/Si(111)-(1x1) prepared by: (a) thermal oxidation followed by etching in buffered HF (pH = 5) for 2 min and subsequent etching in 40%  $\text{NH}_4\text{F}$  for 4 min, and (b) chemical oxidation followed by etching in a 40%  $\text{NH}_4\text{F}$  solution for 6½ min. Both samples are thoroughly rinsed in DI water after the last etching step. (From Ref. 94.)

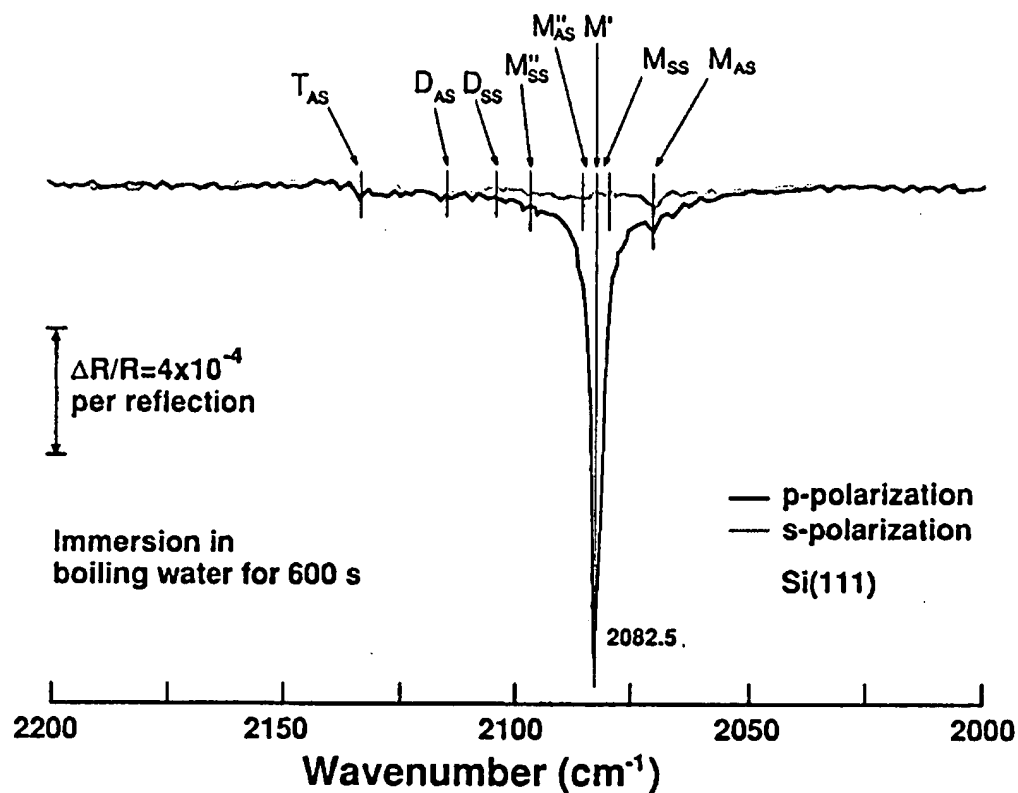
This phenomenon is well known in the literature and is investigated further by treatment in concentrated HF where etching of the H-terminated silicon is minimized. Previous researchers have found that, when a thick thermal oxide ( $\sim 1000 \text{ \AA}$ ) is grown, with post-annealing in an inert gas at the growth temperature ( $\sim 1050^\circ\text{C}$ ), a very smooth Si/SiO<sub>2</sub> interface is formed (3)(30)(104)(105). Dissolution of this oxide in concentrated HF produces a H-terminated Si(111) surface, characterized by a multimode spectrum which indicates atomic roughness (see Fig. 27, top, a). This roughness disappears upon rinsing (see Fig. 27, top, b), as evidenced by the dominance of the monohydride peak afterwards. In contrast, the rough Si(111) surface produced by HF etching of a *chemical* oxide is not removed upon simple rinsing. These observations confirm that the thermally grown oxide has a smoother interface than the chemically grown oxide and suggests that water rinsing alone can remove small surface defects preferentially. Identical experiments were also performed on Si(100) surfaces and are

shown in Fig. 27, bottom. As discussed earlier, the multi-mode spectra imply that the surfaces are atomically rough. Certain spectral changes do occur, however, after rinsing. The monohydride modes decrease in strength while the dihydride modes increase. Note that this is opposite to the behavior observed on Si(111).



**Figure 27.** Top: P-polarized IR absorption spectra of thermally oxidized Si(111) after (a) etching in concentrated HF, and (b) subsequent rinsing in de-ionized water. Bottom: P-polarized IR absorption spectra of thermally oxidized Si(100) after (a) etching in a concentrated HF solution, and (b) subsequent rinsing in de-ionized water.

Preferential etching by water, resulting in flat H-terminated Si(111) surfaces, has recently been demonstrated by Watanabe et al. (1991) (66). These authors studied the effects of water rinsing (65) as a function of water temperature, finding that hot water (100°C) increases the rate of removal of (111) surface defects while maintaining the H-termination. The spectrum obtained is shown in Fig. 28. A single mode, polarized perpendicular to the surface, dominates the spectrum. However, using the analysis developed by Jakob et al. (1991) (77), the spectra indicate that the average domain size is 20 Å, a factor of fifteen smaller than for the sample presented in Fig. 26a. It is surprising that boiling water rinsing did not lead to the growth of a surface oxide. A possible mechanism is discussed in the following section.

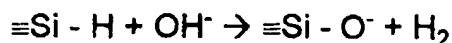


**Figure 28.** Polarized IR absorption spectra of a chemically oxidized Si(111) sample after etching in 1.5% HF solution and subsequent boiling in DI water at 100°C for 10 min. The resolution is 0.5 cm<sup>-1</sup>. (From Ref. 66.)

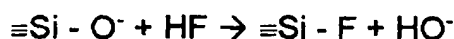
**Mechanism of Preferential Etching.** A solution of concentrated HF dissolves silicon oxide efficiently and passivates the silicon surface with hydrogen. Once hydrogen passivation is achieved, etching stops. As a result, the morphology of the original Si/SiO<sub>2</sub> interface is preserved.



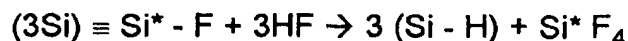
Clearly, the data presented in the previous section indicate that dilution of concentrated HF with water or buffering with ammonium fluoride induces a *slow* etching reaction of the H-passivated silicon surfaces. The overall etch rate increases with the pH of the solution, as evidenced by the increasing formation of small H<sub>2</sub> bubbles as the pH is raised. The bubbles are probably formed during oxidation of the surface by OH<sup>-</sup>, according to the following reaction:



Once oxidized, the surface is subject to HF attack through HF insertion into the Si-O bond, according to the schematic reaction

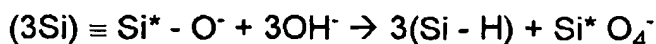


with subsequent removal of the surface Si atom (now labeled Si\* to distinguish it from the underlying bulk Si atoms), and passivation of the second layer silicon atoms by hydrogen, according to the mechanism proposed in Sec. 3.1:



In the above processes, the last two steps are fast compared to the initial oxidation of the H-passivated surface. As a result, the surface is always H-terminated.

The role of OH<sup>-</sup> is clearly a key ingredient in the attack and etching of H-terminated silicon surfaces. It is also important to note that silicon can be etched without HF. Silicon can also be etched with alkaline solutions, such as KOH or NaOH, (106) and even with water (66). These observations indicate that, once oxidized, the silicon surface can be attacked by OH<sup>-</sup>. A plausible reaction pathway involves the silicon back-bond attack by OH<sup>-</sup>:

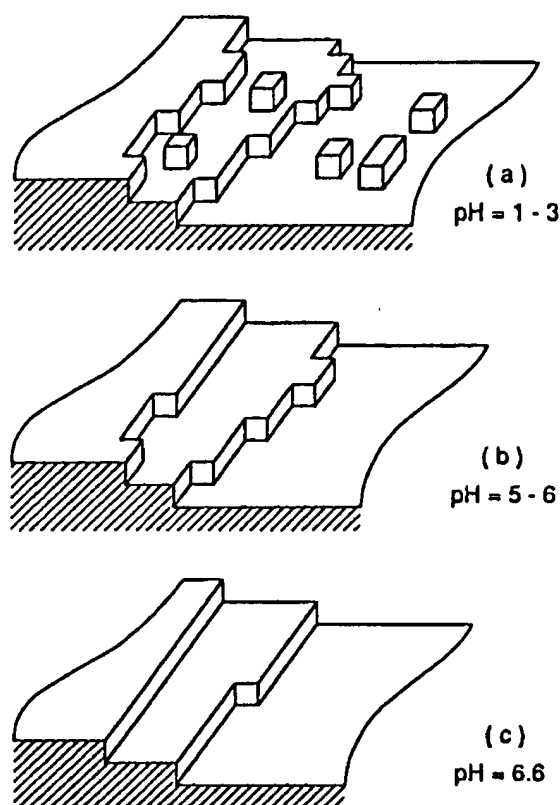


where the last species is actually unstable and decomposes into other soluble products. Confirmation and quantification of the above reaction steps should be possible using first principles cluster calculations, as was done to understand H-passivation of silicon (46). In addition, the influence of surface charges on the anisotropic etching of silicon needs to be understood (107).

The key point in considering *preferential* etching is to realize that oxidation of the H-terminated silicon surface is extremely slow and is the rate-determining step. It takes many collision between  $\text{OH}^-$  ions and the surface Si-H to effect a reaction because the reaction barrier is large. When this is the case, relatively minor factors may affect the reaction probabilities greatly. For instance, if some surface structures are strained, they may be more easily attacked because the reaction barrier is lowered only a small degree. Alternatively, if a surface structure is more accessible for the  $\text{OH}^-$  ion in solution, it may be attacked faster because of an increased reaction probability (larger prefactor).

To understand and quantify the etch rates of various surface structures, the chemical etching of stepped silicon (111) surfaces was studied by Jakob and Chabal (1991) (89) by utilizing IR absorption spectroscopy and STM images to characterize the surface structures after each chemical treatment. The results are summarized in the schematic drawing of Fig. 29 (108). At low pH ( $\text{pH} = 1 - 3$ ), the HF solutions do not modify substantially the original Si/SiO<sub>2</sub> interface which usually displays a fair degree of atomic roughness. The (111) terraces have many small adstructures, and the more extended steps are wandering with a high density of kinks. The IR absorption spectra are very similar to those in Fig. 15 with a relatively low concentration of ideal monohydride termination of the (111) planes. As the pH is increased ( $\text{pH} = 5 - 6$ ), the small adstructures and defects present on the (111) terraces are etched away, leaving atomically flat, ideally monohydride terminated (111) terraces. The step edges, however, remain rough on an atomic scale with a high concentration of kinks. Solutions of higher pH ( $\text{pH} \approx 6.6$ ) are needed to remove kinks and generate atomically straight steps. After three minutes of etching at room temperature, for instance, the steps are straight with a very small (1%) concentration of kinks which is probably accounted for by the imperfection in the azimuth of the miscut.

The above observations indicate a step flow etching mechanism (108)(95). As the pH is increased beyond 7.0, the etching of stepped surfaces increases drastically as evidenced by a large formation of bubbles. The surface then roughens, partly because of increasing fluctuations in the terrace length leading to step bunching, and partly because of the more inhomogeneous conditions at the surface (bubbles, fluctuation in the concentrations of various chemical species, etc.). The result is the formation of large, three-dimensional roughness as evident in STM images (103).



**Figure 29.** Schematic picture of the changes of the Si surface morphology as the etch rate is increased by increasing the pH of the etching solution: (a)  $\text{pH} < 3$ , (b)  $\text{pH} = 5 - 6$ , and (c)  $\text{pH} = 6.6$ . A total etch time of 3 min, including the removal of approx.  $10 \text{ \AA}$   $\text{SiO}_2$ , is assumed. A pH higher than 6.6 leads to step bunching, and therefore to the formation of multiple steps and facets (not shown here).

At a microscopic level, many possible etching mechanisms must be considered. Steric constraints, strain, and bonding configuration can all play a role in determining etch rates. The IR studies of intentionally miscut wafers (89) show that the stability of two types of steps with different bonding configurations and different levels of strain is similar. The unstrained monohydride step, with three Si back-bonds, has an etch rate similar to that of the *strained* dihydride step, with only two back-bonds; and both types of steps remain stable in water. Therefore, the etch rate does not appear to depend strongly on surface strain or on the number of Si back-bonds. On the other hand, the progression summarized in Fig. 29 suggests that the accessibility of surface Si-H entities to  $\text{OH}^-$  ions in solution influences the etch rate directly. To discuss the observations, we use the nomenclature defined in Fig. 19. Isolated trihydrides (labeled T) and "horizontal" dihydrides (labeled D) are removed very efficiently, even by simple rinsing with water (65). Note that such dihydrides are always at the tip of small adstructures and are therefore almost as exposed to  $\text{OH}^-$  ions as isolated

trihydrides. The coupled monohydrides (labeled M) and the "vertical" dihydrides (labeled D') are much more resistant to etching. They are part of bigger adstructures and are therefore less accessible to  $\text{OH}^-$  ions. When coupled monohydrides or dihydrides are part of an extended step, they become even more resistant to etching. Finally, the flat and monohydride terminated (111) planes are the most stable.

The chemistry on these surfaces is obviously complex. The simple mechanisms described above are meant only to give a framework in which to address the problem. They are based solely on HF and  $\text{OH}^-$  chemistry. Surface interactions can also be influenced by species such as  $\text{HF}_2^-$ ,  $\text{H}^+$  and  $\text{NH}_4^+$ . In addition, the differences between  $\text{OH}^-$  and HF are not clearly understood but are being addressed theoretically and experimentally by different approaches.

### 3.3 Contamination Issues

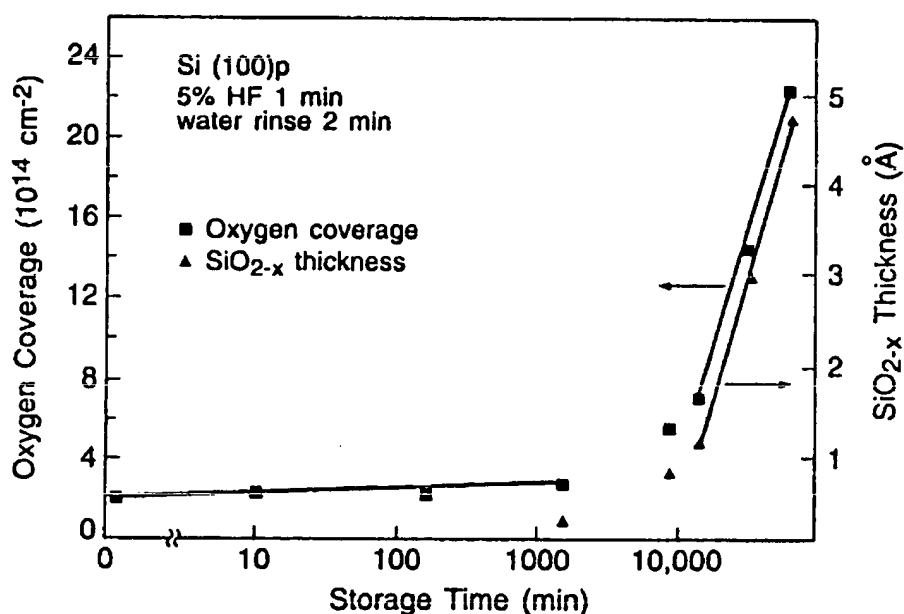
An important contaminant after HF etching is fluorine. Fluorine contamination is the most misunderstood of all the contaminants found on HF etched surfaces. When wafers are treated with concentrated HF without water rinsing, XPS reveals that monolayer quantities of fluorine are present on the surface (50). This could lead to the conclusion that fluorine is the fundamental surface termination responsible for the amazing surface passivation (49). Indeed, fluorine from the HF was identified as playing an important role in reducing the number of defects in gate oxides formed on these surfaces (109). Although there is no doubt that fluorine is present, the form in which it is found and how it is bound to the surface are uncertain. An important experimental result by Gräf et al. (1989) (56) states that rinsing in water strongly reduces surface fluorine concentrations for immersions as short as a few minutes. Surface fluorine concentrations on silicon wafers that were immersed in dilute HF are in the range of a few percent of a monolayer, (55) showing that the surface fluorine concentration can vary vastly. The hydrogen content on the surface, on the other hand, does not vary substantially with rinsing or with HF concentration in the solution. Thus, it is clear that fluorine must be thought of as a surface contaminant rather than the fundamental surface termination.

While it is now generally accepted that the hydrogen termination resulting from HF etching explains the hydrophobicity and the passivation of silicon surfaces, there is still disagreement as to the nature of the fluorine on the surface. It is clear that some of the fluorine must be physisorbed to the hydride covered Si surface in chemical forms, such as HF,  $\text{H}_2\text{SiF}_6$ ,  $(\text{NH}_4)_2\text{SiF}_6$ , or as

ions such as  $F^-$ ,  $HF_2^-$ ,  $SiF_6^{2-}$  (110). The reason for postulating physisorbed species is that the concentration of these contaminants changes greatly with rinsing without changing the surface hydrogen concentration. Thus, physisorbed fluorides can explain many of the observations of fluorine on silicon. All observations of fluorine may not, however, be attributed to physisorbed fluorine, especially after extended rinsing. Many authors believe that some fluorine is directly bonded to substrate Si after HF etching (57)(56)(32)(109). The water rinsing experiments of Gräf et al. (1989) (56) show that fluorine disappears from the surface at the same time that oxygen is taken up by the surface, indicating that an exchange reaction is occurring. Sunada et al. (1990) (32), on the other hand, argue that fluorine termination prevents oxidation until the fluorine concentration falls below a critical value, after which oxidation can proceed normally. Interesting new data suggests that the fluorine is in fact subsurface and only comes to the surface upon oxidation of that surface (39). Clearly, the chemistry of fluorine on the Si surface after HF etching is an important issue still being debated and needs to be studied further.

HF-etched Si surfaces can be prepared to be oxygen free. As mentioned above, however, oxygen concentrations are found to grow as a result of prolonged water rinsing (56)(32). The atomically flat Si(111) wafers produced by etching in  $NH_4F$ , on the other hand, are amazingly resistant to oxidation and show negligible amounts of oxygen after water rinses as long as 10 min (61). The conclusion from this result is that the oxidation rate must somehow be related to the step density on the surface. This might lead to the conclusion that  $H_2O$  or  $OH^-$  attack the step edges more readily and lead to oxidation, but the boiling in water experiments of Watanabe et al. (1991) (66) suggest otherwise. Their surfaces are found to be terminated completely with hydrogen, with little if any residual oxygen, demonstrating that step edge attack in water does not necessarily lead to oxide formation. Oxidation appears to be more complex than simple attack by water. Oxidation in liquid solution has been found to be related to the oxygen concentration in the water used during the rinsing process as well as the doping type of the wafers used (31). It is interesting to note that lightly doped wafers can be rinsed for  $10^4$  min without appreciable oxide growth when water with a low  $O_2$  concentration is used. Further research regarding this issue is certainly warranted. Oxidation due to storage in air is also of current interest. Gräf et al. (1990) (111) have reported that wafers stored in standard moist air (relative humidity 35 - 40%), oxidize extremely slowly, growing less than 1 Å of oxide in seven days ( $10^4$  min) (Fig. 30). After seven days of storage the oxidation rate increases abruptly, with the oxide

thickness approaching 10 Å after forty-five days. This bimodal oxidation rate distribution is not understood at this time but has been observed in other work (31)(32) and has been postulated to be related to the fluorine coverage on the surface (32). It should be noted that hydrogen-terminated surfaces have been prepared that show less than a monolayer of oxygen after seven days of storage both in air (111) and in water (31), given the fact that many researchers still believe that the growth of native oxide begins immediately. The cleanliness of the chemicals available at the time may have influenced the observed oxidation rates, leading to the erroneous conclusion that the oxide growth was an intrinsic rather than extrinsic effect.



**Figure 30.** Oxygen coverage (left scale) and oxide thickness (right scale) as a function of storage time in moist air. Oxygen coverage was determined by x-ray photoelectron spectroscopy. (From Ref. 114.)

Hydrocarbon contamination is a particularly insidious problem for hydrogen-terminated HF treated wafers. Whereas hydrophilic oxide-passivated surfaces are relatively resistant to hydrocarbon contamination, H-terminated Si surfaces can be covered with a monolayer of hydrocarbons extremely quickly if exposed to a contaminated environment. Hydrocarbon contamination can come from the water rinse used (57), from contaminants in laboratory air, or from the environments of processing equipment. Infrared spectra have shown that H-terminated Si samples, prepared in dilute HF and rinsed in high-quality water, transported through air and

loaded into a nitrogen purged vacuum chamber remain hydrocarbon free, only to be contaminated the second one begins evacuating the chamber (112). In fact, clean surfaces have been preserved only in the case where the load locks of the analysis chambers were pumped down to a few times  $10^{-10}$  torr prior to venting for sample introduction (90)(61). It is obvious that these surfaces are highly sensitive to hydrocarbons and become contaminated unless extreme precautions are taken (55)(57). Part of the problem is that many common contaminants desorb at temperatures above the hydrogen desorption temperature (113). When this happens silicon carbides are formed and are impossible to remove at reasonable temperatures. In contrast, hydrocarbons on top of oxide coated surfaces can be made to desorb before the oxide desorbs. Oxide passivation is obviously preferred if the 850 - 950°C desorption temperatures can be tolerated (37).

Metal contamination is also of crucial importance and is discussed in other chapters of this book. In brief, wafers etched in HF following the RCA standard clean can be free of metal contamination ( $<10^{10} \text{ cm}^{-2}$ ) (4). In other instances, however, Cu was found to be a problem and was eliminated by adding some  $\text{H}_2\text{O}_2$  to the HF (5). Cu has been found to be extremely detrimental to the stability of the H-termination by causing increased oxidation rates during water rinses, resulting in 3 Å of oxide growth in just 2 min (114). This reaction has been attributed to Cu-catalyzed oxidation (114) of the Si, which causes bulk etching and surface roughness (5) upon exposure to contaminated HF solutions. Cu coverages of up to a half a monolayer are obtained on exposure to HF solutions contaminated with only ppm levels of Cu (114). Copper in HF is known to plate out on semiconductor surfaces; the use of ultrapure HF (and other reagents) in semiconductor processing is, therefore, imperative (1)(12).

#### 4.0 SUMMARY AND FUTURE DIRECTIONS

Two distinct types of surface cleans for silicon wafers have been discussed. The first leaves a thin chemical oxide behind and the second results in a hydrogen-terminated silicon surface. Both techniques are extremely effective at cleaning and passivating the Si surface. Three major issues were discussed for each of these classes of cleans: chemical composition, structure and morphology, and contamination issues.

The composition of chemically grown oxides on silicon surfaces is similar to that of the interfacial transition regions of thermally grown oxides. The oxides are largely composed of  $\text{SiO}_2$  containing a fraction of sub-oxide

species, dominated by  $\text{Si}^{2+}$ . The largest intrinsic contaminant found on such surfaces is hydrogen-bonded OH and  $\text{H}_2\text{O}$ . Minor levels of hydrogen in the form of Si-H are also observed. The structure and morphology of chemomechanically polished silicon wafers approaches atomic perfection with a surface roughness of 2 Å rms. The SC-1 clean is found to increase levels of surface roughness, whereas the Piranha and SC-2 cleans tend to leave surface topographies unchanged. The oxide interfacial structure is found to vary with preparation technique with the indication that the chemically grown oxide interfaces are substantially rougher than their thermal oxide counterparts. Extrinsic contaminants, such as metals and hydrocarbons, are efficiently removed using RCA cleaning, but there is an increasing concern that the  $10^{10} \text{ cm}^{-2}$  level achieved for most metals today will have to be improved in the future. Other areas where future work is necessary include: gaining an understanding of how contaminants in the solutions used influence etching and surface topography; elucidating the mechanism of chemical oxidation in the various solutions employed; and learning, finally, how to control the surface structure and composition of oxide-terminated silicon surfaces.

Hydrogen-terminated silicon surfaces are composed of hydrogen atoms covalently bonded to the substrate wafer. The electronic perfection of this interface is unsurpassed, indicating an extremely low dangling bond density. Fluorine is now understood to be a minor constituent of the surface and is one of the major intrinsic contaminants observed. The mechanism of H-termination involves back-bond attack by HF molecules that is facilitated by the charge transfer caused by Si bonding to highly electronegative elements, such as fluorine or oxygen. Si(100) and Si(111) surfaces are found to be atomically rough when etched in concentrated or dilute HF. This result was originally inferred by the coexistence of many types of silicon-hydrides on the surface and was later confirmed using a variety of techniques. High-pH HF solutions lead to increased roughness on Si(100) with the formation of microfacets, but can produce atomically smooth Si(111). These ideally monohydride-terminated Si(111) surfaces have been characterized by use of a variety of surface science techniques, demonstrating the surface quality which can be achieved using solution chemistry alone. Such surfaces allow highly detailed studies which can be used to elucidate the fundamental mechanisms of etching. In this regard,  $\text{OH}^-$  has been identified as being responsible for the anisotropic etching observed. Surprisingly, water rinsing alone can also be used to achieve a certain level of atomic perfection on Si(111) surfaces and leads to the conclusion that anisotropic etching can occur in rinsing operations. Hydro-



gen-terminated silicon surfaces are particularly susceptible to hydrocarbon contamination and extreme precautions must be taken in order for this contaminant to be avoided. H-terminated surfaces have been prepared which are essentially metal free ( $<10^{10} \text{ cm}^{-2}$ ), but solutions contaminated with Cu must be avoided when using HF. Recent findings indicate that the growth of native oxide occurs much more slowly than previously believed. Researchers find that silicon wafers remain essentially oxide free for up to seven days in both in air and water. Future work should be focused on understanding the role of fluorine on these surfaces and the chemistry of HF and  $\text{OH}^-$  in these solutions. Understanding the role of metal contaminants in HF solutions is also of critical importance. Learning to control Si(100) surface chemistries and morphologies at a level similar to that achieved for Si(111) will be of greatest importance.

The foundation of the advances made in our understanding of these surfaces comes not only from old techniques, such as infrared absorption spectroscopy, but also from several newer experimental tools, such as the scanning tunneling microscope, the atomic force microscope, or high-resolution electron energy loss spectroscopy and high-resolution x-ray photoelectron spectroscopy. Furthermore, new theoretical techniques, such as first principles molecular orbital calculations of chemical activation barriers have provided a quantitative basis for understanding important surface chemical reactions. In this chapter, we have stressed not only the technology of wet chemical cleaning, but have tried to emphasize the science behind the wet chemistry. This area of research is growing rapidly and we hope that better understanding will be central to successful semiconductor processing in the future.

## ACKNOWLEDGMENTS

It is a pleasure to acknowledge our long time collaborators in this work, R. S. Becker, P. Dumas, and K. Raghavachari. We would also like to thank V. A. Burrows, P. Jakob, and G. W. Trucks, for stimulating discussions and their contributions to our present understanding of this problem. P. Jakob deserves special thanks for providing many of the IR spectra used in this manuscript. Thanks also go to M. A. Hines, I. K. Robinson, and J. E. Rowe for critical reading of this manuscript. S. B. Christman, E. E. Chaban, A. J. Becker, and R. D. Yadvish are also gratefully acknowledged for their technical support.

## REFERENCES

1. Kern, W., *J. Electrochem. Soc.* 137:1887 (1990)
2. Buck, T. M., and McKim, F. S., *J. Electrochem. Soc.*, 105:709 (1958)
3. Hahn, P. O. and Henzler, M., *J. Vac. Sci. Technol.* A2:574 (1984)
4. Heyns, M., Hasenack, C., De Keersmaecker, R., and Falster, R., *Proc. of the 1st Int. Symp. on Cleaning Technology in Semiconductor Device Manufacturing*, (J. Ruzyllo and R. E. Novak, eds.), PV 90-9:293 Electrochemical Society, Pennington, NJ, (1990)
5. Ohmi, T., Miyashita, M. and Imaoka, T., *Proc. of the Microcontamination Meeting*, San Jose, CA, p. 491, Canon Communications, (October 16-18, 1991)
6. Atalla, M. M., Tannenbaum, E. and Scheibner, E. J., *Bell System Tech. Journal*, 38:749 (1959)
7. *The Physics of SiO<sub>2</sub> and Its Interfaces*, (S. T. Pantelides, ed.) Pergamon Press, NY (1978)
8. *The Physics and Chemistry of SiO<sub>2</sub> and the Si-SiO<sub>2</sub> Interface*, (C. R. Helms and B. E. Deal, eds.) Plenum Press, NY (1988)
9. Nicollian, E. H. and Brews, J. R., *MOS (Metal Oxide Semiconductor) Physics and Technology*, Wiley-Interscience, NY (1982)
10. Grunthaner, F. J. and Maserjian, J., *IEEE Trans. on Nuclear Science*, NS 24:2108 (1977)
11. Ourmazd, A. and Bevk, J., in *The Physics and Chemistry of SiO<sub>2</sub> and the Si-SiO<sub>2</sub> Interface*, (C. R. Helms and B. E. Deal, eds.), p. 189, Plenum Press, NY (1988)
12. Kern, W. and Puotinen, D., *RCA Rev.* 31:187 (1970)
13. Deal, B. E. and Kao, D.-B., *Proc. of the 1986 Tungsten and Other Refractory Metals for VLSI Applications II*, (E. K. Broadbent, ed.), p. 27, Materials Research Society, Pittsburgh, PA (1987)
14. Mikata, Y., Inoue, T., Takasu, S., Usami, T., Ohta, T., Hirano, H., *Proc. of the 1st Int. Symp. on Si Molecular Beam Epitaxy*, (J. C. Bean, ed.), p. 45, Electrochemical Society, Pennington, NJ (1990)
15. Ogawa, H., Terada, N., Sugiyama, K., Moriki, K., Miyata, N., Aoyama, T., Sugino, R., Ito, T. and T. Hattori, *Appl. Surf. Sci.*, 56-58:836 (1992)
16. Sugiyama, K., Igarashi, T., Moriki, K., Nagasawa, Y., Aoyama, T., Sugino, R., Ito, T. and Hattori, T., *Jpn. J. Appl. Phys.*, 29:L2401 (1990)
17. Yablonovitch, E. and Gmitter, T. J., "Diagnostic Techniques for Semiconductor Materials and Devices," *Fall ECS* (1988)

18. Kiselev, A. V. and Lygin, V. I., *Infrared Spectra of Adsorbed Species* (L. H. Little, ed.), pp. 213, 228, Academic Press, NY (1966)
19. Schaefer, J. A., Frankel, D. J., Stucki, F., Göpel, W. and Lapeyre, G. J., *Surf. Sci.* 139:L209 (1984)
20. Nagasawa, Y., Ishida, H., Takayagi, T., Ishitani, A. and Kuroda, H., *Solid-State Electronics*, 33:129 (1990)
21. Hahn, P. O., Grundner, M., Schnegg, A. and Jacob, H., *The Physics and Chemistry of SiO<sub>2</sub> and the Si-SiO<sub>2</sub> Interface*, (C. R. Helms and B. E. Deal, eds.), p. 401, Plenum Press, NY (1988)
22. Schnegg, A., Lampert, I. and Jacob, H., *Electrochemical Society (ECS) Extended Abstracts*, 85-1:394, Toronto (1985)
23. Ourmazd, A., Taylor, D. W., Rentschler, J. A., and Bevk, J., *Phys. Rev. Lett.*, 59:213 (1987)
24. Green, M. P., Hanson, K. and Higashi, G. S., to be published.
25. Mishima, H., Yasui, T., Mizuniwa, T., Abe, M. and Ohmi, T., *IEEE Trans. Of Semiconductor Manufacturing*, 2:69 (1989)
26. Miyashita, M., Itano, M., Imaoka, T., Kawanabe, I. and Ohmi, T., *Technical Digest of the 1991 Symp. on VLSI Technology*, Oiso, Japan, p. 45., (May 28-30, 1991)
27. Ohmi, T., Kotani, K., Teramoto, A., and Miyashita, M., *IEEE Electron Dev. Lett.*, 12:652 (1991)
28. Ohmi, T., Miyashita, M., Itano, M., Imaoka, T. and Kawanabe, I., *IEEE Trans. on Electron Dev.*, 39:537 (1992)
29. Verhaverbeke, S., Meuris, M., Mertens, P. W., Heyns, M. M., Philipossian, A., Gräf, D. and Schnegg, A., *Proc. Int. Electron Devices Meeting*, p. 71 (1991)
30. Gibson, J. M., Lanzerotti, M. Y. and Elser, V., *Appl. Phys. Lett.*, 55:1394 (1989)
31. Morita, M., Ohmi, T., Hasegawa, E., Kawakami, M., and Suma, K., *Appl. Phys. Lett.*, 55:562 (1989)
32. Sunada, T., Yasaka, T., Takakura, M., Sugiyama, T., Miyazaki, S. and Hirose, M., *Ext. Abstracts of the Conf. On Solid State Devices and Materials*, Sendai, p. 1071 (1990)
33. Heyns, M., Hasenack, C., De Keersmaecker, R. and Falster, R., *Microelectronic Engineering*, 10:235 (1991)
34. Ohsawa, A., Honda, K., Takizawa, R., Nakanishi, T., Aoki, M. and Toyokura, N., *Semiconductor Silicon 1990*, (H. R. Huff and K. G. Barraclough, eds.), p. 601, Electrochemical Society, Pennington, NJ (1990)

35. Murrell, M., Sofield, C., Sugden, S., Verhaverbeke, S., Heyns, M. M., Welland, M. and Golen, B., *Proc. Silicon Ultra-Clean Processing Workshop*, Oxford (Sept. 1991)
36. Henderson, R. C., *J. Electrochem. Soc.*, 119:772 (1972)
37. Ishizaka, A., Nakagawa, K. and Shiraki, Y., *Second Int. Symp. on MBE and Clean Surface Related Techniques*, (R. Ueda, ed.), Jpn. Soc. of Applied Physics, Tokyo, p. 183 (1982)
38. Vig, J. R., *J. Vac. Sci. and Technol.*, A3:1027 (1985)
39. Kasi, S. R., Liehr, M. and Cohen, S., *Appl. Phys. Lett.*, 58:2975 (1991)
40. Beckmann, K. H., *Surf. Sci.*, 3:314 (1965)
41. Shinn, N. D., Morar, J. F. and McFeely, F. R., *J. Vac. Sci. and Technol.*, A2:1593 (1984)
42. Harrick, N. J. and Beckmann, K. H., *Characterization of Solid Surfaces*, (P. F. Kane and G. B. Larrabee, eds.), p. 243, Plenum Press, NY (1974)
43. Ubara, H., Imura, T. and Hiraki, A., *Solid. State Comm.*, 50:673 (1984)
44. Imura, T., Mogi, K., Hiraki, A., Nakashima, S. and Mitsuishi, A., *Solid State Comm.*, 40:161 (1981)
45. Miyasato, T., Abe, Y., Tokumura, M., Imura, T. and Hiraki, A., *Jpn. J. Appl. Phys.*, 22:L580 (1983)
46. Trucks, G. W., Raghavachari, K., Higashi, G. S. and Chabal, Y. J., *Phys. Rev. Lett.* 65:504 (1990)
47. Raider, S. I., Flitsch, R. and Palmer, M. J., *J. Electrochem. Soc.* 122:413 (1975)
48. Licciardello, A., Puglisi, O. and Pignataro, S., *Appl. Phys. Lett.* 48:41 (1988)
49. Weinberger, B. R., Deckman, H. W., Yablonovitch, E. Gmitter, T., Kobasz, W. and Garoff, S., *J. Vac. Sci. Technol.* A3:887 (1985)
50. Weinberger, B. R., Peterson, G. G., Eschrich, T. C. and Krasinski, H. A., *J. Appl. Phys.* 60:3232 (1986)
51. Yablonovitch, E., Allara, D. L., Chang, C. C., Gmitter, T. and Bright, T. B., *Phys. Rev. Lett.* 57:249 (1986)
52. Grunthaner, F. J. and Grunthaner, P. J., *Mat. Sci. Reports*, 1:65 (1986)
53. Grunthaner, P. J., Grunthaner, F. J., Fathauer, R. W., Lin, T. L., Hecht, M. H., Bell, L. D., Kaiser, W. J., Schowengardt, F. D. and Mazur, J. H., *Thin Solid Films* 183:197 (1989)
54. Grundner, M. and Jacob, H., *Appl. Phys.* A39:73 (1986)

55. Grundner, M. and Schulz, R., *AIP Conf. Proc. No. 167*, (G. W. Rubloff and G. Lucovsky, eds.), American Institute of Physics, pp. 329-337, NY (1988)
56. Gräf, D., Grundner, M. and Schulz, R., *J. Vac. Sci. Technol.* A7:808 (1989)
57. Takahagi, T., Nagai, I., Ishitani, A., Kuroda, H. and Nagasawa, Y., *J. Appl. Phys.* 64:3516 (1988)
58. Burrows, V. A., Chabal, Y. J., Higashi, G. S., Raghavachari, K. and Christman, S. B., *Appl. Phys. Lett.* 53:998 (1988)
59. Chabal, Y. J., Higashi, G. S., Raghavachari, K. and Burrows, V. A., *J. Vac. Sci. Technol.* A7:2104 (1989)
60. Fenner, D. B., Biegelsen, D. K. and Bringans, R. D., *J. Appl. Phys.* 66:419 (1989)
61. Dumas, P. and Chabal, Y. J., *Chem. Phys. Lett.*, 181:537 (1991)
62. Dumas, P., Chabal, Y. J. and Jakob, P., *Surf. Sci.*, 269/270:867 (1992); Dumas, P. and Chabal, Y. J., *J. Vac. Sci. Technol.* A10:2160 (1992)
63. Judge, J. S., *J. Electrochem. Soc.* 118:1772 (1971)
64. Novak, R. E., *Solid State Technol.*, p 39., (March 1988)
65. Higashi, G. S., Chabal, Y. J., Trucks, G. W. and Raghavachari, K., *Appl. Phys. Lett.* 56:656 (1990)
66. Watanabe, S., Nakayama, N. and Ito, T., *Appl. Phys. Lett.* 59:1458 (1991)
67. Bauer, E., *Ultramicroscopy*, 17:51 (1985); Teliëps, W. and Bauer, E., *Ultramicroscopy*, 17:57 (1985)
68. Henzler, M., *Topics in Current Physics: Electron Spectroscopy for Surface Analysis*, (H. Ibach, ed.) 4:117, Springer, Berlin (1977); Henzler, M., *Advances in Solid State Physics*, (J. Treusch, ed.) (Festkörperprobleme X, Vieweg, 1979) p. 193; Henzler, M., *Surf. Sci.* 36:109 (1973)
69. Robinson, I. K., *Phys. Rev.* B33:3830 (1986)
70. Robinson, I. K., Waskiewicz, W. K., Tung, R. and Bohr, J., *Phys. Rev. Lett.* 57:2714 (1986)
71. Klitsner, T., Becker, R. S. and Vickers, J. S., *Phys. Rev.* B41:3837 (1990)
72. Becker, R. S., Swartzentruber, B. S., Vickers, J. S. and Klitsner, T., *Phys. Rev.* B39:1633 (1989)
73. Doak, R. B., Single Phonon Inelastic Scattering, in *Atomic and Molecular Beam Methods*, Vol.II, (G. Scoles, ed.), Ch. 14, p. 384, Oxford Univ. Press, NY (1991)

74. Ibach, H. and Mills, D. L., *Electron Energy Loss Spectroscopy and Surface Vibrations*, p. 94, Academic Press, London, (1982)
75. Chabal, Y. J., *Surf. Sci. Reports* 8:211 (1988)
76. Ibach, H., *Electron Energy Loss Spectrometers, The Technology Of High Performance*, Springer Verlag, Berlin (1991)
77. Jakob, P., Chabal, Y. J., and Raghavachari, K., *Chem. Phys. Lett.* 187:325 (1991). Note that the analyses were carried out for isolated domains. For adjacent domains, as is the case for real surfaces, the fits must be re-normalized leading to  $N = 2 \times 10^4$  Si-H units (i.e., 600 Å domains).
78. Collins, R. J. and Fan, H. Y., *Phys. Rev.* 93:674 (1954)
79. Harrick, N. J., *Internal Reflection Spectroscopy* (Wiley, NY (1967); Second printing by Harrick Scientific Corporation, Ossining, NY (1979)
80. Olsen, J. E. and Shimura, F., *Appl. Phys. Lett.* 53:1934 (1988); *J. Appl. Phys.* 66:1353 (1989)
81. Sawara, K., Yasaka, T., Miyazaki, S. and Hirose, M., *Proc. Int. Workshop on Science and Technol. for Surface Reaction Process*, p. 93, Tokyo (Jan. 22-24, 1992)
82. Richardson, H. H., Chang, H-C., Noda, C. and Ewing, G. E., *Surf. Sci.* 216:93 (1989)
83. Hahn, P. O., *Mat. Res. Soc. Symp. Proc.* 54:645 (1986)
84. Schaefer, J. A., Stucki, F., Frankel, D. J., Göpel, W. and Lapeyre, G. J., *J. Vac. Sci. Technol.* B2:359 (1984)
85. Chabal, Y. J. and Raghavachari, K., *Phys. Rev. Lett.* 54:1055 (1985). The frequency associated with the isolated vibrations of the dihydrides,  $2111 \text{ cm}^{-1}$  at room temperature on HF etched Si(100), is substantially different from that of the corresponding dihydride mode on the UHV prepared H/Si(100),  $2096 \text{ cm}^{-1}$  at room temperature. In addition, the similarity between the dihydride spectra of Fig. 18 in p- and s-polarization clearly indicates that the dihydrides are inclined with respect to the surface normal. It is not surprising, therefore, that the modes associated with the strained monohydride (anti-symmetric =  $2087 \text{ cm}^{-1}$  and symmetric =  $2099 \text{ cm}^{-1}$ ) are absent in the spectra of the chemically prepared Si(100). These two observations clearly show that the chemically prepared Si(100) surfaces are not atomically flat. Also, no spectral feature can be ascribed to an ideal dihydride termination of the surface as suggested by Grundner and Schulz from EELS data, in Ref. 55. In fact, calculations have shown that the strain associated with an "ideally" dihydride terminated surface would render it unstable.

86. Dumas, P., Chabal, Y. J., and Higashi, G. S., *Phys. Rev. Lett.* 65:1124 (1990)
87. Kobayashi, H., Edamoto, K., Onchi, M. and Nishijima, M., *J. Chem. Phys.* 78:7429 (1983)
88. Froitzheim, H., Kolher, U. and Lammering, H., *Surf. Sci.* 149:537 (1985)
89. Jakob, P. and Chabal, Y. J., *J. Chem. Phys.*, 95:2897 (1991)
90. Morita, Y., Miki, K. and Tokumoto, H., *Appl. Phys. Lett.* 59:1347 (1991)
91. Morita, Y., Miki, K. and Tokumoto, H., *Ultramicroscopy* (May 1992); Morita, Y., Miki, K. and Tokumoto, H., *Jpn.. J. Appl. Phys.*, 30:3570 (1991)
92. Uram, K. J. and Jansson, U. *Surf. Sci.* 249:105 (1991)
93. Higashi, G. S., Becker, R. S., Chabal, Y. J. and Becker, A. J., *Appl. Phys. Lett.* 58:1656 (1991)
94. Jakob, P., Dumas, P. and Chabal, Y. J., *Appl. Phys. Lett.* 59:2968 (1991)
95. Hessel, H. E., Feltz, A., Reiter, M., Memmert, U. and Behm, R. J., *Chem. Phys. Lett.* 186:275 (1991)
96. Becker, R. S., Higashi, G. S., Chabal, Y. J. and Becker, A. J., *Phys. Rev. Lett.* 65:1917 (1990)
97. Kim, Y. and Lieber, C. M., *J. Am. Chem. Soc.* 113:2333 (1991)
98. Miglio, L., Ruggerone, P., Benedek, G. and Colombo, L., *Physica Scripta* 37:768 (1988)
99. Doak, R. B., Chabal, Y. J., Higashi, G. S. and Dumas, P., *J. Electron Spectr. Related Phenomena* 54/55:291 (1990)
100. Harten, U., Toennies, J. P., Wöll, C., Miglio, L., Ruggerone, P., Columbo, L. and Benedek, G., *Phys. Rev.* B38:3305 (1988)
101. Stuhlmann, C., Bogdanyi, G and Ibach, H., *Phys. Rev.*, B45:6786 (1992)
102. Guyot-Sionnest, P., Dumas, P., Chabal, Y. J. and Higashi, G. S., *Phys. Rev. Lett.* 64:2156 (1990)
103. Becker et al., to be published.
104. Hahn, P. O. and Henzler, M., *J. Appl. Phys.* 52:4122 (1981)
105. Ogura, A., *J. Electrochem. Soc.* 138:807 (1991)
106. Holmes, P. J., *The Electrochemistry of Semiconductors*, (P. J. Holmes, ed.), p. 329, Academic Press, London (1962)

107. Seidel, H., Csepregi, L., Heuberger, A. and Baumgärtel, H., *J. Electrochem. Soc.*, 137:3626 (1990)
108. Jakob, P., Chabal, Y. J., Raghavachari, K., Becker, R. S. and Becker, A. J., and *Surf. Sci.*, 275:407 (1992)
109. Yu, B.-G., Arai, E., Nishioka, Y., Ohji, Y., Iwata, S. and Ma, T. P., *Appl. Phys. Lett.*, 56:1430 (1990)
110. Yota, J. and Burrows, V. A., *Mat. Res. Soc. Symp. Proc.*, 204:345 (1991); Yota, J. and Burrows, V. A., *J. Appl. Phys.*, 69:7369 (1991)
111. Gräf, D., Grundner, M., Schulz, R. and Mühlhoff, L., *J. Appl. Phys.*, 68:5155 (1990)
112. Hydrocarbon content was measured by infrared absorption before and after evacuation.
113. Kasi, S. R., Liehr, M., Thiry, P. A., Dallaporta, H. and Offenber, M., *Appl. Phys. Lett.*, 59:108 (1991)
114. Gräf, D., Grundner, M., Mühlhoff, L. and Dellith, M., *J. Appl. Phys.*, 69:7620 (1991)